Introduction of Error Correcting Schemes in the Design Process of Self-Healing Circuits for Nanoscale Fabrics

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Introduction

On the road of smaller nanoscale devices perspectives, new proposals of alternatives to CMOS technology are emerging for nanoscale fabrics. This paper relies on a specific 2D-grid nanowire fabric and proposes new CAD tool to help the designer in its nanoscale implementation, from high-level specification to abstract layout. This tool proposes to incorporate some fault-tolerant techniques at different levels of the design process (functional level and structural level). The layout of the defect-tolerant circuit can be produced in a semi-automatic way based on the fault-tolerance directives given to the tool.

This paper focuses on a framework for designing self-healing circuits for a specific nanofabric (NASIC fabric), by incorporating error-correcting schemes into synthesis process. Even if the study is done for a specific nanofabric, the framework proposed, here, could be enlarged to other 2D-grid nanoscale fabrics.

NASIC fabric and defects

NASICs[1][4] are based on FETs formed at the crosspoints of perpendicular semiconductor nanowires(NWs). In NASICs, NWs are self-assembled to build a crossbar structure using some aligning techniques, e.g., fluidic alignment. FETs can be selectively formed at NW crosspoints in a tile for a certain function. The basic building blocks for NASICs are nanotiles, nanoarrays surrended by macrowires(MWs). Nanotiles in NASICs are based on either static ratioed or dynamic logic blocks, using 2-level AND-OR logic (Pla style). MWs are used to provide power, ground signals and the control signals for different logic style to nanoarrays. One key constraint is that the NWs have unique doping in each dimension on the grid. For example, all NWs in one dimension are doped as N-type while all perpendicular NWs are doped as P-type.

Self-assembly techniques would likely add other types of defects than top-down lithography. For example, in a process that requires the metallization of segments connecting transistors, the channels of transistors are more likely to be metallized over (and therefore stuck-on) than stuck-off (meaning the channel is always off). In NASICs three main types of defects are considered: NWs may be broken, the transistors at the crosspoints may be stuck-on or stuck-off.

Error-correction strategies in NASIC fabrics

To handle defects at nanoscale, two solutions can be proposed: reconfiguration or built-in fault tolerance. NASIC fabric use built-in fault tolerant techniques to generate the self-healing logic. The main advantage of these ones is the reduction of the complexity of the micro-nano interface that is usually involved in a solution based on reconfiguration. Built-in tolerant techniques introduce two general kinds of redundancy: structural redundancy with replication of horizontal and vertical NWs and devices at crosspoint, and code redundancy with built-in error-correcting circuitry. Code redundancy generalizes the use of error-correcting codes (like Hamming, or BCH code) for nanofabric. The additional logic due to the error-correcting code or structural replication can mask a large number of defects when combining with a pull-up/pull-down circuitry.

Prototyping framework for nanofabric

To help the designer in his nanoscale implementation, we use Madeo Framework[2]. This framework provides us a good prototyping context including nanofabric modeling and synthesis process from behavioral description. The general flow of Madeo framework was adapted to nanoscale fabric as presented in figure 1. In this flow, fault-tolerant options that can be introduced in the synthesis process on designer demands. Physical tools utilize a abstract nanoscale fabric model including model of Fet devices, nanowires, microwires and some topological information (regular structures of 2D grids). These tools, initially devoted to FPGA style, were modified to incorporate NASIC fabric features (place-route adapted to VLSI style organization and specific control signals for dynamic logic style design).

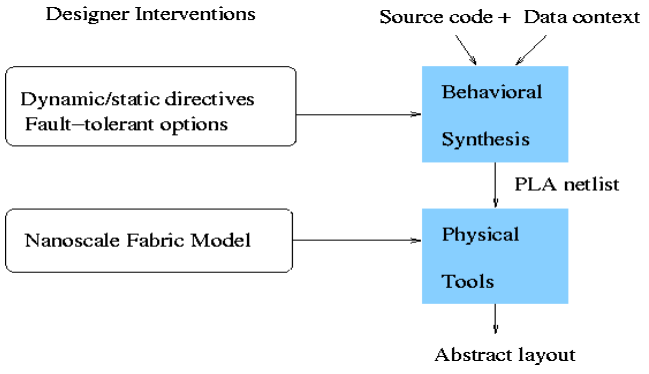

Figure 1: Madeo framework for nanofabric

Error-correction schemes taken into account

To generate self-healing logic, different types of transformations are proposed during the design process (for the 'behavioral synthesis' stage of Madeo). These are organized around the core logic synthesis process (realized by an external tool, Espresso[3]) at different levels. Error-correcting schemes are introduced: at functional level with additional typing to introduce EC codes (BCH codes are used) and at structural level (after the logic synthesis) to introduce some structural duplications. Both of them are shown in figure 3, respectively corresponding to transformation (a) and transformation (c). The transformation introducing complementary inputs and outputs (transformation (b)) provides some redundancy but are necessary for the type of logic defined for the nano-grid.

After applying these transformations, the result produced is a netlist of defect-tolerant Plas that can be placed and routed using physical tools of Madeo. The yield quality of the implementation can be controlled by a yield simulator (external tool[4]) and if the yield is not satisfactory, it is possible to do some iterations with different error-correction schemes applied individually on each nodes of the initial Dag.

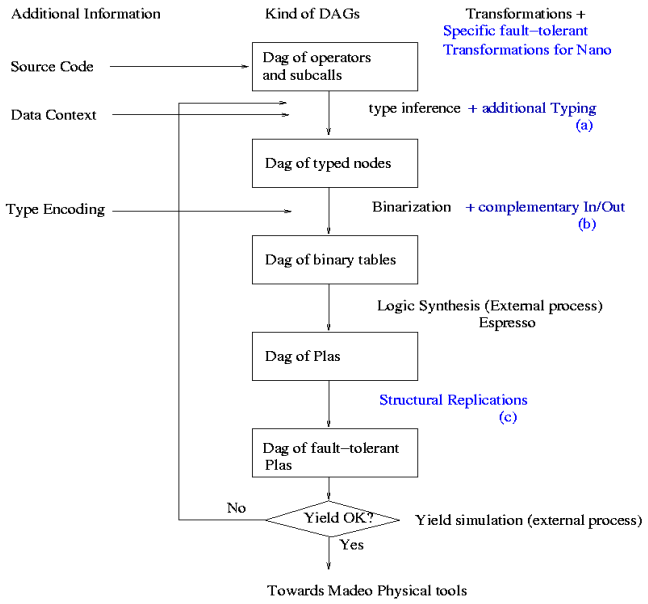

Figure 2: Introduction of error-correction schemes in 'behavioral synthesis' flow of Madeo framework

Layout production

Wisp0 [1][4] is a 2-bit processor example that exercises different different types of techniques developed for NASIC fabrics. We show in figure 3, one example of abstract layout of the circuit Wisp0 produced by Madeo , defined on several tiles. This design includes error correcting techniques (EC codes and structural redundancy) in the first tile. This production can give us an idea of the organization of the WISP0 circuit on a regular structure.

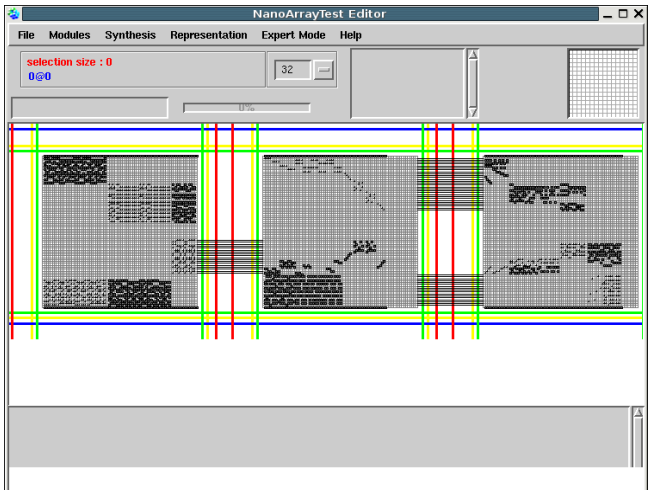

Figure 3: One possible layout of partial defect-tolerant WISP0 produced by Madeo

Future work

This paper focuses on design tool for a specific nanofabric (NASIC fabric). This tool gives an overview on how specific defects due to the fabrication process could be taken into account in the synthesis process of CAD tool to produce self-healing logic. Several techniques like specific typing (use of error-correcting codes) and structural replications are considered. The strategy of choosing one of these techniques can be determined depending on the surface, the performance, the power and the defect-tolerance of the layout produced. For now, the proposed tool can investigate different solutions considering area criterion and some defect-tolerance criteria. Further versions should define a more complete CAD tool incorporating more error-correcting schemes and better interface to the yield simulator(more tightly coupled to physical tools) to help the designer in his investigation for larger designs.

References

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