

# Dependable Multiprocessing with the Cell Broadband Engine

Dr. David Bueno, Dr. Matt Clark, Dr. John R. Samson, Jr.  
Honeywell Inc., Space Electronic Systems

[david.bueno@honeywell.com](mailto:david.bueno@honeywell.com), [matthew.clark@honeywell.com](mailto:matthew.clark@honeywell.com), [john.r.samson@honeywell.com](mailto:john.r.samson@honeywell.com)

Adam Jacobs

[jacobs@hcs.ufl.edu](mailto:jacobs@hcs.ufl.edu)  
University of Florida

## Introduction

As processing requirements for space exploration, space science, and defense missions continue to outgrow the current state-of-the-art in radiation-hardened technology, a critical need is developing to apply commercial-off-the-shelf (COTS) processors to space-based computing. Dependable Multiprocessor (DM) technology is a high-performance, highly dependable, portable, fault-tolerant framework for space-based cluster computing that enables the use of COTS-based processing technology in space. In this paper, we explore the application of DM technology to systems including the IBM/Sony/Toshiba Cell Broadband Engine™ (Cell BE) processor.

## Dependable Multiprocessor

A paper describing the DM project through its Technology Readiness Level 5 (TRL5) validation was presented at HPEC 2006 [1], and the DM flight experiment is on schedule to take place from March-September 2009. This work extends the DM framework to a “next-generation” prototype test bed with PowerPC 970FX-based platforms and Cell Processor Development Systems (CPDSs).

## Cell BE Architecture

The Cell Broadband Engine is a multi-core, heterogeneous architecture that has shown much promise for high-performance embedded applications. First-generation Cell architectures contain a single 64-bit Power Processing Element (PPE), as well as up to eight Synergistic Processing Elements (SPEs) that are highly optimized for compute-intensive applications [2]. Under a typical Cell BE programming model, the PPE serves as an orchestrator, handing tasks to the SPEs, whose jobs are to process the data and return results to the PPE as quickly as possible. Communication between the SPEs and PPE occurs using an explicit DMA-based model, with the application programmer responsible for moving data in and out of the “local store” of each SPE. In the case of the current-generation Cell processors, this local store is a 256 KB “scratchpad” memory. The benefit of this approach is extremely deterministic SPE performance and increased control over system memory access patterns.

## Integration of DM and Cell Technology

Honeywell is currently integrating Dependable Multiprocessor technology into a “next-generation” heterogeneous system consisting of multiple Cell processors and PowerPC 970FX processors. Figure 1

shows the Honeywell CPDS/970FX cluster with four, dual-processor PowerPC 970FX-based Momentum Computer systems running Debian GNU/Linux 4.0, and four Sony PlayStation 3 CPDSs running Fedora Core 6 Linux. The Sony PlayStation®3 (PS3) presents a very cost-effective platform for evaluation of Cell technology and prototyping of applications, offering much of the performance of higher-end Cell-based systems with many times the cost. The key drawbacks to this approach are a limited amount of system memory (256 MB XDR RAM), and a reduced number of SPEs available in PS3 hardware (six) compared to Cell hardware specifically designed for high-performance computing (eight).

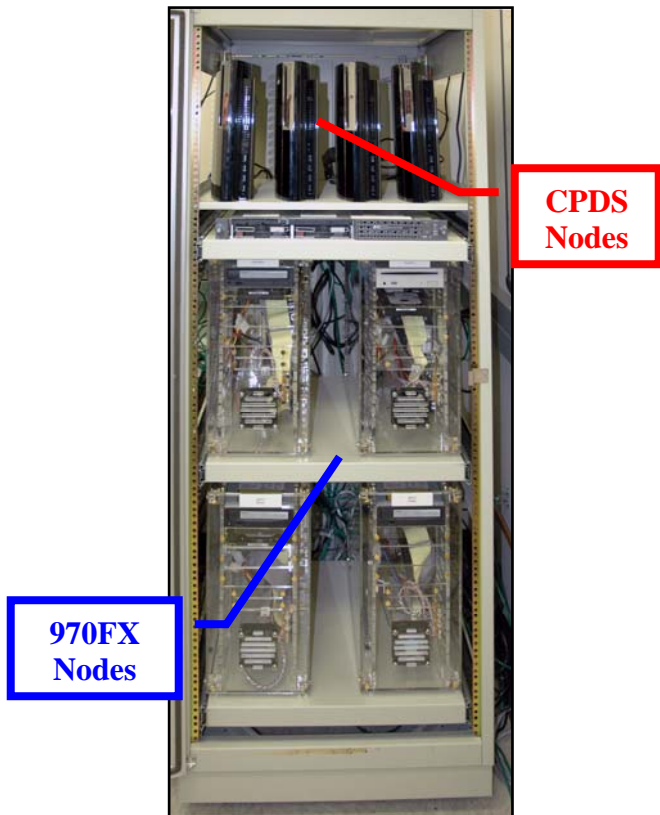


Figure 1- Honeywell CPDS/970FX Cluster

Because DM technology is architecture-independent and portable, it can run on the PPE of the Cell processor, causing the Cell processor to appear as a “conventional” processor to the other system nodes and abstracting the Cell’s multi-core architecture at the system level. The poster will detail the integration of DM technology with the Cell and 970FX processors, and will present performance- and dependability-related results for several applications

running on the next-generation DM cluster. Future work may explore the adaptation of DM to other platforms, including next-generation Polymorphous Computing Architectures (PCAs) or the AFRL/IT Floating Point Application Specific Processor (FPASP).

## References

- [1] J. Samson, et al., "Dependable Multiprocessing (DM)," 10<sup>th</sup> High Performance Embedded Computing Workshop, M.I.T. Lincoln Laboratory, September 20, 2006.
- [2] J. Kahle, et al., "Introduction to the Cell Multiprocessor," *IBM Journal of Research and Development*, Vol. 49, No. 4/5, July/September 2005, pp. 589-604.