Gedae

HPEC 2007: Multicore Processors and Their Impact on DoD HPEC Systems

Gedae Portability: From Simulation to DSPs to the Cell Broadband Engine

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The Software Architecture Makes Hardware Refreshes Difficult

PE-2 PE-0 PE-1 PE-3 Old System Code Code Code Code 0 2 3 New System Code Code Code Code Code Code B Ε С D F Α **PE-B PE-C PE-D PE-A** PE-E **PE-F**

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Problems that Reduce Software Portability



- Languages and compilers are based on serial processors
- Software architecture is buried in the code
- Differences in multiprocessor/multicore hardware necessitate changes to the software architecture
 - Number of processors
 - Interconnection
 - Bandwidth
 - Processor speed
 - Memory size
 - Memory structure
- Gedae mitigates the risk of porting software by automating the incorporation of the software architecture

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Application Environment

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Search and track using four audio channels
 Display using camera directed by pan-tilt unit



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Stages in Development

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Developed as simulation with file input and rendered output Deployed on quad PowerPC board, processing in real time at limited frame rate

Hardware refresh to Cell Broadband Engine processor, processing more frames per second

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System Specifications

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	Simulation	Mercury AdapDev	Playstation 3
Processors	1	4 PowerPC AltiVec (500 MHz), 1 Pentium	1 PPE, 6 SPEs
Sensors	Datafile of 4 recorded channels	ICS 610 ADC PCI Board, 4 microphones	M-Audio Quattro USB Device, 4 microphones
Output	Constellation display	Directed Perception D46-17 Pan-Tilt Unit	Directed Perception D46-17 Pan-Tilt Unit
UI	Rendered scene	Matrix Vision BlueFOX USB Camera displayed using Video for Gedae	Matrix Vision BlueFOX USB Camera displayed using Video for Gedae
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Algorithm Specified in Gedae

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Simulation Using Gedae-Sim

🚆 m_disp.m_disp

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- Audio data captured from actual model train, recorded to file
- Simulated 3-d environment created with train, track, camera, and light
- Scene rendered from vantagepoint of camera
 Gedae-Sim used to verify algorithm
 - and run on multiple virtual processors

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Spot Formation Output

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Mercury AdapDev

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Pentium III development host

- 1.26 GHz
- 1 GB SDRAM
- Quad PowerPC 500MHz (MCP7410)
 - AltiVec instruction set
 - 2 MB L2 cache
 - 256 MB SDRAM
 - DMA engines
- RACE++ switched-fabric architecture



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Mercury AdapDev Implementation

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Cell/B.E. Architecture

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SPE

LS

DMA

- **Power Processing Element (PPE)**
- 8 Synergistic **Processing Elements** (SPE)
 - VMX SIMD instruction set
 - DMA engines
 - 256 kB Local Storage (LS)
- System Memory

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- **Element Interconnect** Bus (EIB)
 - Over 200 GB/s

SPE SPE SPE SPE SPE LS LS IS S DMA DMA DMA DMA DMA DMA DMA **Element Interconnect Bus Bus interface** PPE Memory controller controller

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Cell/B.E. Implementation

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- Gedae was used to easily move the application to new hardware
- Changes to the implementation were handled by automation and simple GUIs, not changes to code
- High performance gains were realized with minimal effort

Target	Programmer Hours	Performance
Simulation	4 weeks	-
Mercury AdapDev	6 hours	3 Hz
Cell/B.E.	2 hours	15 Hz

