DARPA STAP-BOY:

Fast Hybrid QR-Cholesky Factorization and Tuning Techniques for STAP Algorithm Implementation on GPU Architectures

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STAP-BOY: Concept

Problem:

- Complex sensor modalities and algorithms needed for smaller platforms (SAR, 3D-motion video, STAP, SIGINT, ...)
- Low-cost platform constraints limit real-time on-board/offboard and distributed sensing algorithms and performance
- Timely distribution, visualization, and processing of mission-critical data not available to tactical decision makers
- STAP-BOY Goal:
- Develop low-cost, scalable, teraflop, embedded multi-modal sensor processing capability based on COTS graphics chips

STAP-BOY Approach:

- Map complex algorithms to COTS graphics chips with open source graphics languages
- Prototype scalable, parallel, embedded computing architecture for handhelds to teraflop single card
- Demonstrate on available, tactically representative sensor systems



Constant Hawk Advanced EO/IR Processor 100Mpixel camera, 10 GPUs (10kmx10km, 1m)





Applications Pull



CPUs vs. GPUs



Intel® quad-core QX6700



NVIDIA® 8800 GTX

582 million	Transistors	681 million
2.66 GHz	Clock Speed	1.35 Ghz
4	# of Cores	128
Serial	Programming Model	Highly parallel
Minimize latency	Design Goal	Maximize throughput
Complex cores: • Branch prediction • Out-of-order execution	Design Approach	Simple cores: • Smaller caches • In-order execution
43 GFLOPS	Theoretical Max. Computation Rate	346 GFLOPS

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- Requires geometry set-up to perform computation
- -Vertex shaders needed to get data into pixel shaders
- -More complex graphics programming model
- Shader memory access controlled by OpenGL -Hidden copies and cache control limit pixel shader FLOP performance

- - Eliminates complicated graphics programming concepts
 - Exposes hardware as a data-parallel processor array
 - Simplified programming model
- · Direct programming and memory management

Source: "A Performance-Oriented Data Parallel Virtual Machine for GPUs," Segal, M., and Peercy, M. ACM SIGGRAPH Sketch, 2006.

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Outline

- Algorithms that take advantage of the highly parallel nature of the GPU programming model can run significantly faster than on CPUs
 - Radar STAP
 - > Weight Solver:
 - Covariance method is more parallelizable than QR
 - Sliding window algorithm results in additional speed-up
 - > STAP beamforming: matrix-matrix multiply is fast on GPU
 - Spin Images
 - Spin-image matching component: parallel over model and scene points, reduction over image pixels
 - Geometric consistency component: parallel over pairs of point correspondences
 - SAR/Tomography
- Continuing advances in GPU hardware and stream software will enable single chip solutions for a large class of STAP airborne applications and similarly sized problems





Productivity



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Weight Solver Methods



Covariance matrix method yields identical mathematical solution to QR and exploits 2-D matrix operations in a highly parallel fashion



Shared-row Covariance Method: Algorithm Steps



• Estimate covariance matrix of the shared rows (6:12)

 $C_s = \sum_{l=6}^{12} \frac{1}{6} A_l A_l^T$ where A_l is a snapshot vector

If covariance matrix is block Toeplitz

$$C_{s} = \sum_{l=6}^{12} \frac{1}{6} A_{l(1:n)} A_{l(1:n/k)}^{T}$$

Compute Cholesky factorization of shared-row covariance matrix

 $C_s = L_s L_s^T$ where L_s is lower triangular

• Update Cholesky Factors using shared row method (derived on next slide)

$$\begin{bmatrix} L_{(4:12)} \\ 0 \end{bmatrix} = H \begin{bmatrix} L_s \\ A_{(4)} \\ A_{(5)} \end{bmatrix} \qquad \begin{bmatrix} L_{(5:13)} \\ 0 \end{bmatrix} = H \begin{bmatrix} L_s \\ A_{(5)} \\ A_{(13)} \end{bmatrix} \qquad \begin{bmatrix} L_{(6:14)} \\ 0 \end{bmatrix} = H \begin{bmatrix} L_s \\ A_{(13)} \\ A_{(14)} \end{bmatrix}$$

H can be a sequence of Givens or Householder rotations Now we have computed the following Cholesky factors:

$$C_{(4:12)} = L_{(4:12)}L_{(4:12)}^{T} \qquad C_{(5:13)} = L_{(5:13)}L_{(5:13)}^{T} \qquad C_{(6:14)} = L_{(6:14)}L_{(6:14)}^{T}$$



Shared-Row Covariance Method: Low-Rank Updates



H can be a sequence of Givens or Householder rotations

Modification from Golub and Van Loan, 1996

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Total Speedup for the STAP Algorithm



Over 64-Bit State-of-the-Art CPUs

Interpreting Range with Spin-Image Mapping





Spin-Image Surface Mapping

Spin-image Matching

- For each sample scene point, compare to all model points
- Match using image correlation
- Geometric consistency
 - Find pairs of point correspondences with best spin-coordinate match
- Transformations
 - Best pair of point correspondences determines a transformation that maps the model into the scene





Parallel Processing Opportunities

- Spin-image matching component
 - Image-correlation-based statistic
 - > Parallel over model and scene points
 - > Reduction over image pixels
 - > O(W*H*P*M*S) for WxH spin-image at P model points on each of M models with S sample scene points
- Geometric consistency component
 - Coordinate match statistic
 - > Parallel over pairs of point correspondences
 - > O(M*N²) for N point correspondences for each of M models



Achieving Speedup

• Offload explicitly parallel portions to the GPU

- > Spin-image correlation
- > Spin-image coordinate matching
- Bulk of processing time (Time Reduction regime)
- Only 2 times -3 times speedup

Address less obvious parallelizations

- Geometric consistency thresholding
- Where not fully parallelizable in current API, then do minimal amount on CPU and utilize GPU/CPU shared memory to reduce data transport.
- Eliminated most of remaining serial time (Transition regime)
- 8 times 11 times speedup

• Consolidate code on GPU to minimize data upload/download

- Small reductions in overall time gave large increases in speedup (Data Throughput regime)
- 20 times 24 times speedup



GPU Speedup & Timing



- Graphics card: ATI™ X1900 XTX
 - 48 pixel shaders @ 640 MHz
 - GPU Memory 512 MB
 - GPU Memory bandwidth 1550 MHz
- CPU: Xeon® 2800 MHz
- Comms: PCI Express®
 - 250 MB/s each direction, per lane
 - 16 lanes: 4 GB/s

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Additional results



STAP-BOY Signal Processing Implementations Demonstrated Almost Two Order Magnitude Speedup over State-of-the-Art CPU with Three-Week Development Cycles



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