FPGA Based Systolic Array Implementation of QR Transformation Using Givens Rotations

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Givens Rotation Algorithm:

$$\begin{bmatrix} c & -s \\ s & c \end{bmatrix}^T \begin{bmatrix} a \\ b \end{bmatrix} = \begin{bmatrix} r \\ 0 \end{bmatrix}$$

$$r = \sqrt{a^2 + b^2}$$

c: cosine

s: sine

function: $[c, s] =$ **givens**(a, b)

if $b = 0$

$c = 1; s = 0$

else

if $|b| > |a|$

$\tau = a/b; s = 1/\sqrt{1+\tau^2}; c = s\tau$

else

$\tau = b/a; c = 1/\sqrt{1+\tau^2}; s = c\tau$

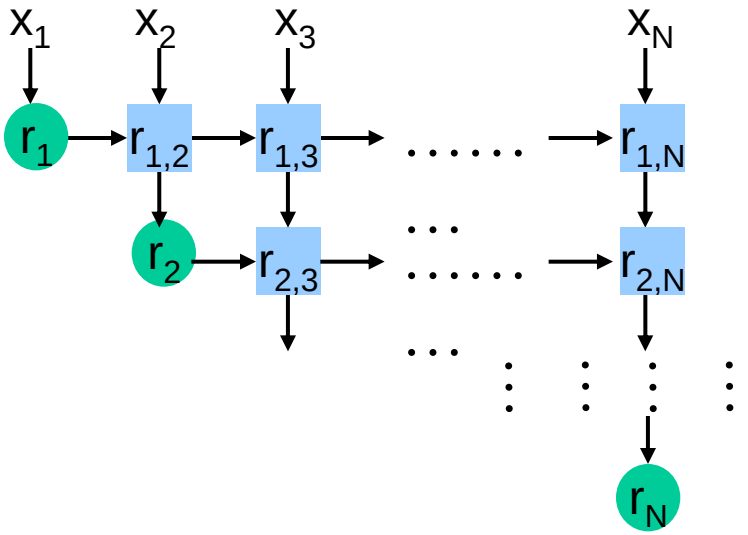
end

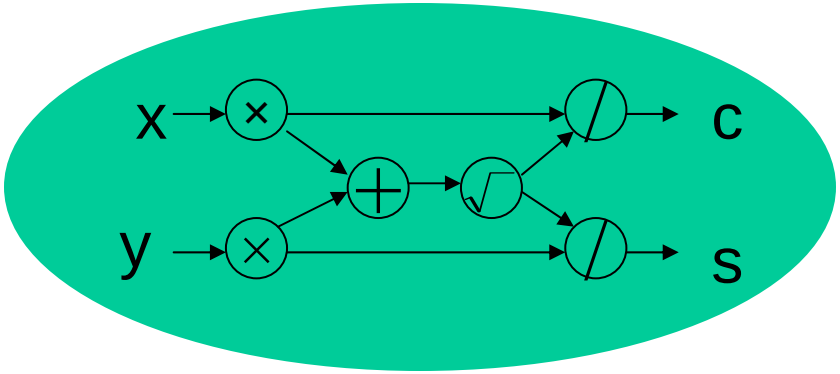
end

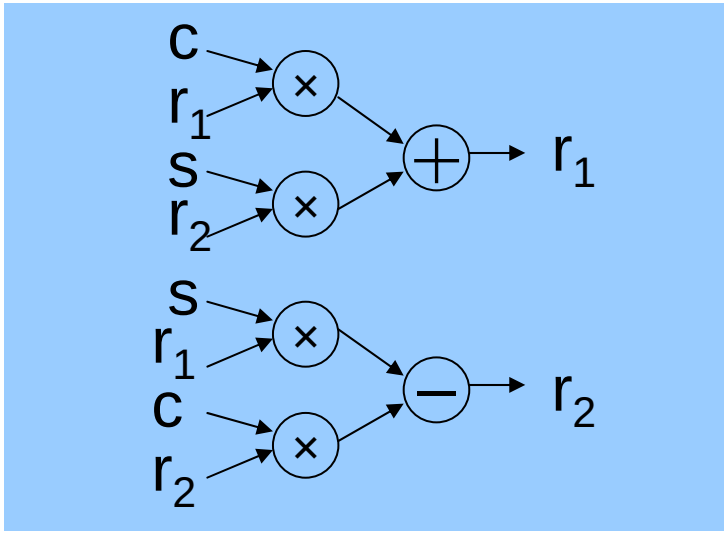
end givens

- **Divide and square root are required**

2D Systolic Array Architecture for QR Implementation





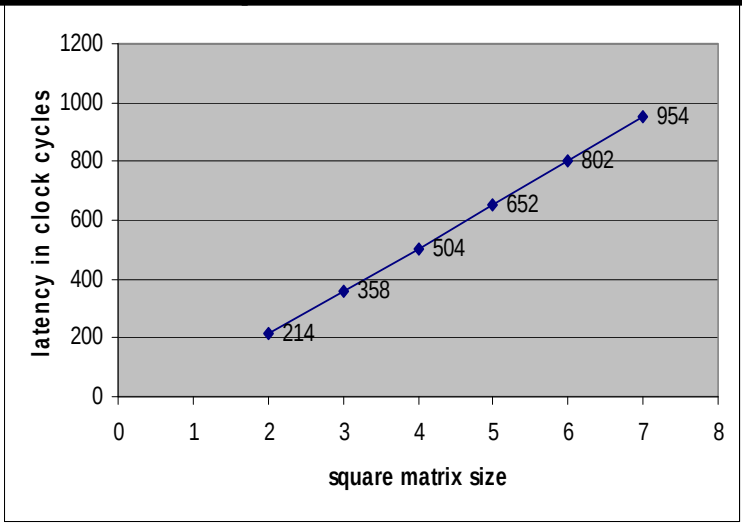


- **Diagonal PE: calculate the rotation parameters c and s**
- **Off-diagonal PE: update the matrix elements using rotation parameters**

Experimental Results

Resources and Speed: XC5VLX220

Format	Matrix Size	Slices	BlockRAMs	DSPs	Latency (cycles)	Frequency (MHz)
32(8,23)	7x7	126585	56	102	954	132
24(8,11)	12x12	120094	30	106	335	139



Latency
IEEE Single-precision square matrix

- **1D implementation: 1302 cycles**
- **Our 2D implementation: 954 cycles**
- **2D latency increases linearly with matrix size, scales well for larger matrices**