Digital Beam Former Coefficient Management Using Advanced Embedded Processor Technology

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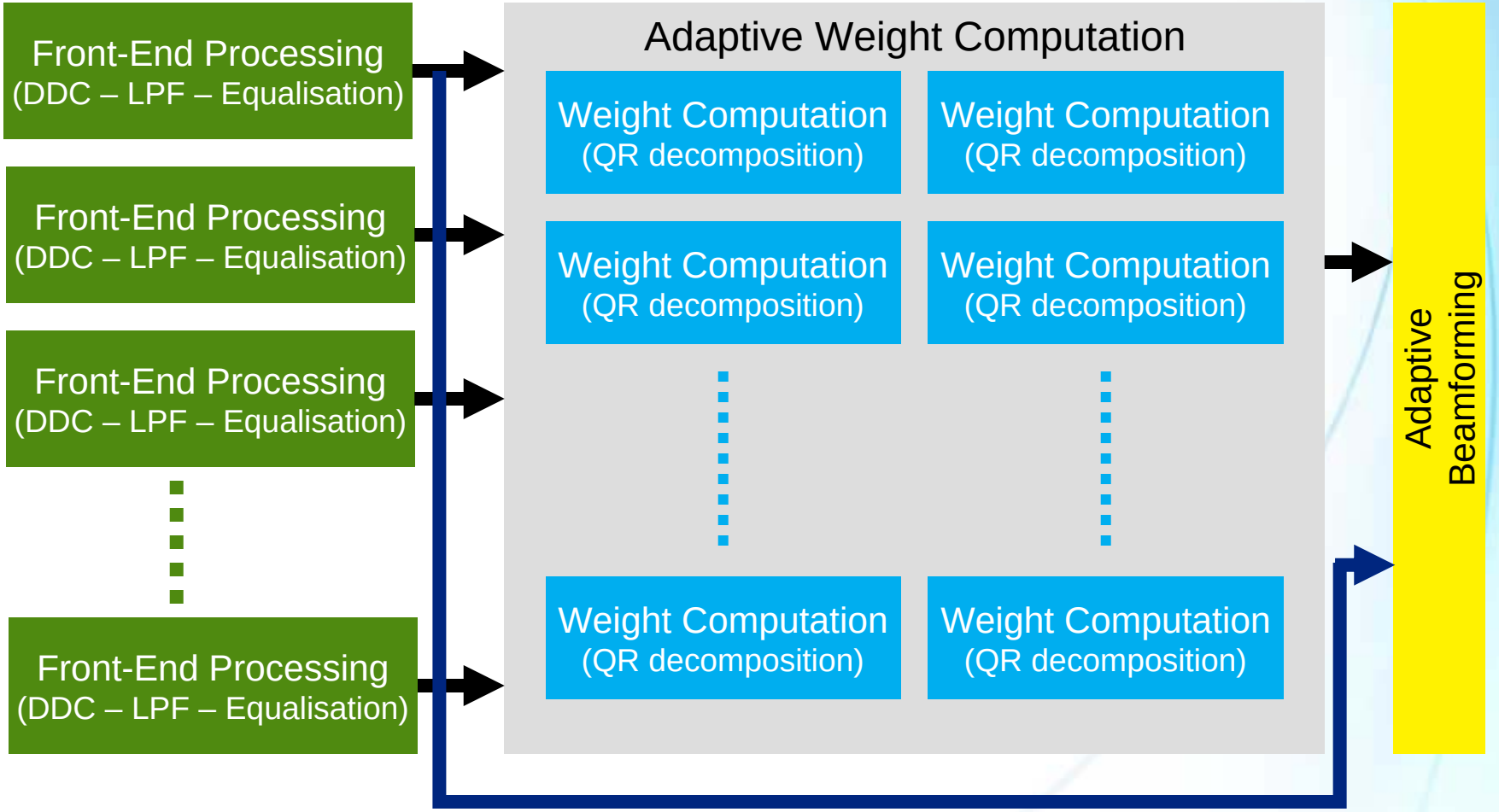
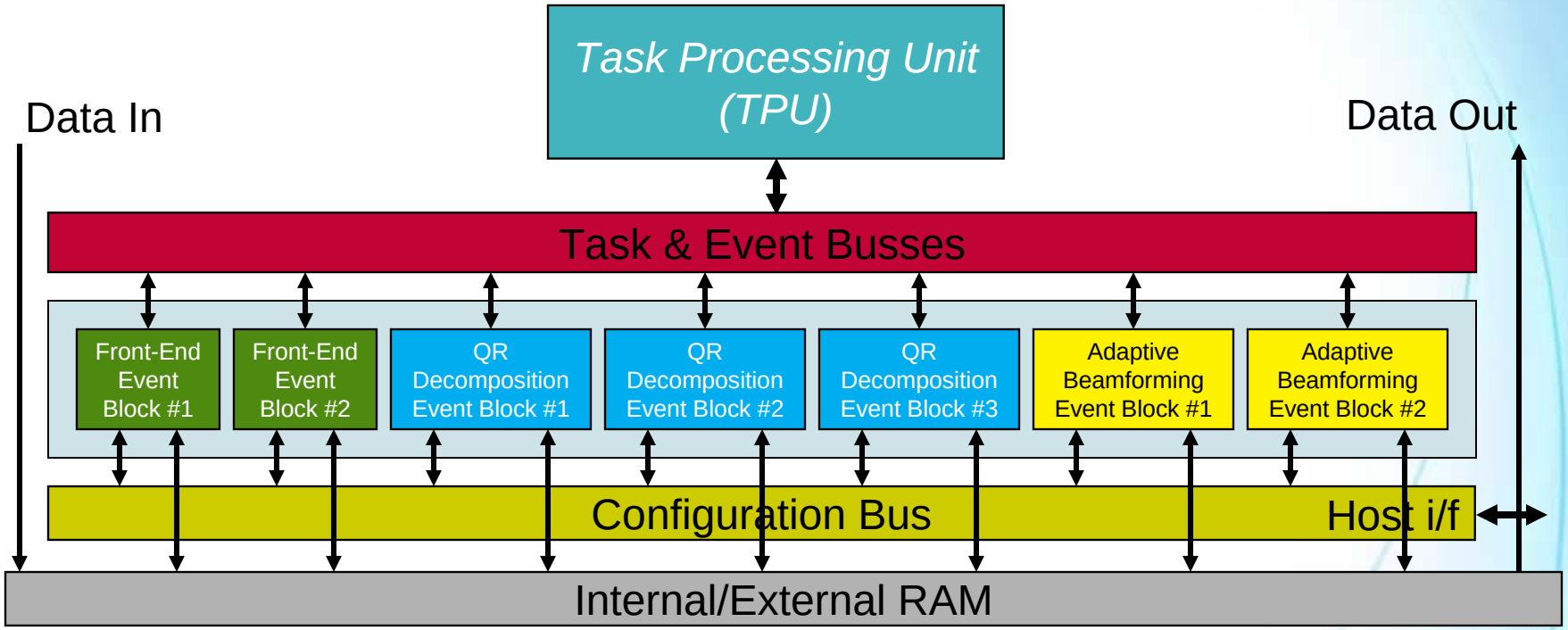
Typical Beamforming Scenario



PicaRisc Beamforming Architectural Solution



PicaRisc Architecture is a Multi-Thread Soft Processor

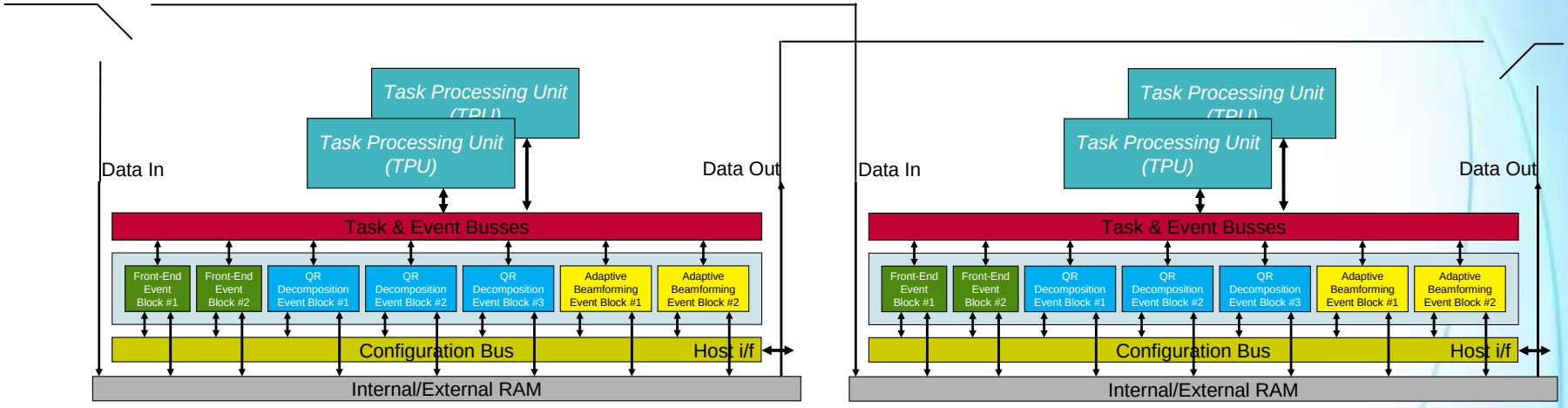
- Intended to assume tasks of general purpose processor (less heat, less power)
- Reduces bottlenecks normally found with embedded RISC processors
- Routes and executes DSP subroutines

PicaRisc tools include

- Compiler, Assembly Support, and Debug GUI

Using PicaRisc in Radar Processing

Scalable in two ways: multiple Task Processing Units, and multiple data flows



PicaRisc has been implemented in non-military products:

- Communications infrastructure (packet routing, header processing)
- Imaging, image processing (scalable bandwidth)
- Can be targeted to Hard Copy™ Structured ASIC device

PicaRisc implementation and performance has been benchmarked at:

- 200-400 MHz in several 90 nm FPGA parts
- Roughly 700 Logic Elements for PicaRisc, and 400 per Task Processing Unit

STILL highly confidential technology – contact Altera for details under NDA