Digital Beam Former Coefficient Management Using Advanced Embedded Processor Technology

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Overview

Modern digital beam forming (DBF) radar systems utilize weighted coefficients among hundreds of radiating elements to create beams, nulls, and optimized sidelobe patterns. Because of the technology-driven increase in the number of elements, sampling rates, and fast-adaptive beam forming algorithms, beam weighting calculations have been mostly managed and switched with pipelined FPGA hard logic. However, by utilizing new advances in FPGA embedded processors, it is possible to increase algorithmic flexibility and make rapid "software decisions" in the digital front end.

The technology behind this enhanced embedded processor is in the release process by Altera Corporation.

Digital Receiver Description

The digital receiver of a RADAR system is made up of several common components somewhat independent of architecture. These include analog receive elements, analog-to-digital conversions, digital filtering and waveform adaptation, and digital beam forming.

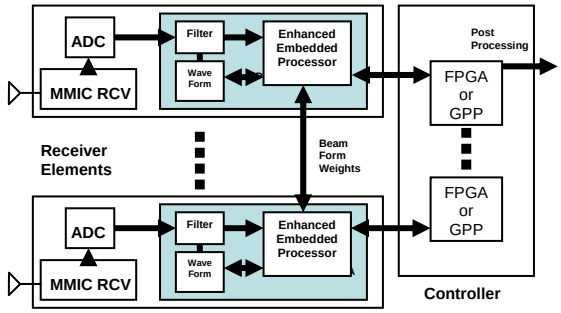

Figure 1: Representative Digital Receiver

The digital beam forming network is a series of weighted additions of the signals received by each receiver element. The decision making process for these beam forming networks are performed in several different ways, but increasingly are made with streamlined hardware decisions within FPGA logic.

The trade-off between digital beam adaptability and high-speed operation is the heart of the digital beam forming design space.

Using newer flexible RISC processing technology, tailored algorithms for digital beam forming can be implemented that overcome the instruction "bottleneck" problems associated with traditional RISC processors.

Advanced RISC Processing

Altera's new multi-threaded, scalable, high performance RISC embedded processor is called 'PicaRisc'. It is currently used for applications in packet processing and imaging. Examples of applications for digital signal processing and digital beam forming networks will be demonstrated with sample architectures.

PicaRisc has been tested and benchmarked on several FPGA's. It takes about 700 logic elements for PicaRisc, plus 400 per Task Processing Unit (TPU). More than one TPU can be compiled in a PicaRisc chain. Performance has been benchmarked between 200 and 400 MHz, depending on chip and application.

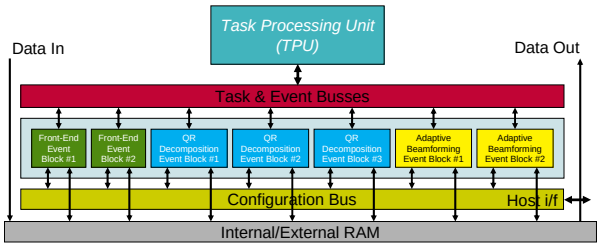

Figure 2: Advanced Embedded Processor Architecture (PicaRisc)

Several advantages can be realized with software-based decisions in the digital front end. Simple electronic warfare countermeasures can be implemented with fast reaction times (handful of cycles). Waveform adaptation tactics can be spread among front-end and back-end decision chains based on required reaction times.

Summary

The capabilities of this embedded technology have been proven for several commercial customers with high-speed packet routing requirements, and Altera systems engineers have targeted several important new applications. This paper aims to show the application of the new embedded processor capabilities to the domain of radar and sensor signal-processing system designers.