Prototyping Advanced Military Sensor Systems Using FPGA-to-ASIC Design Flow

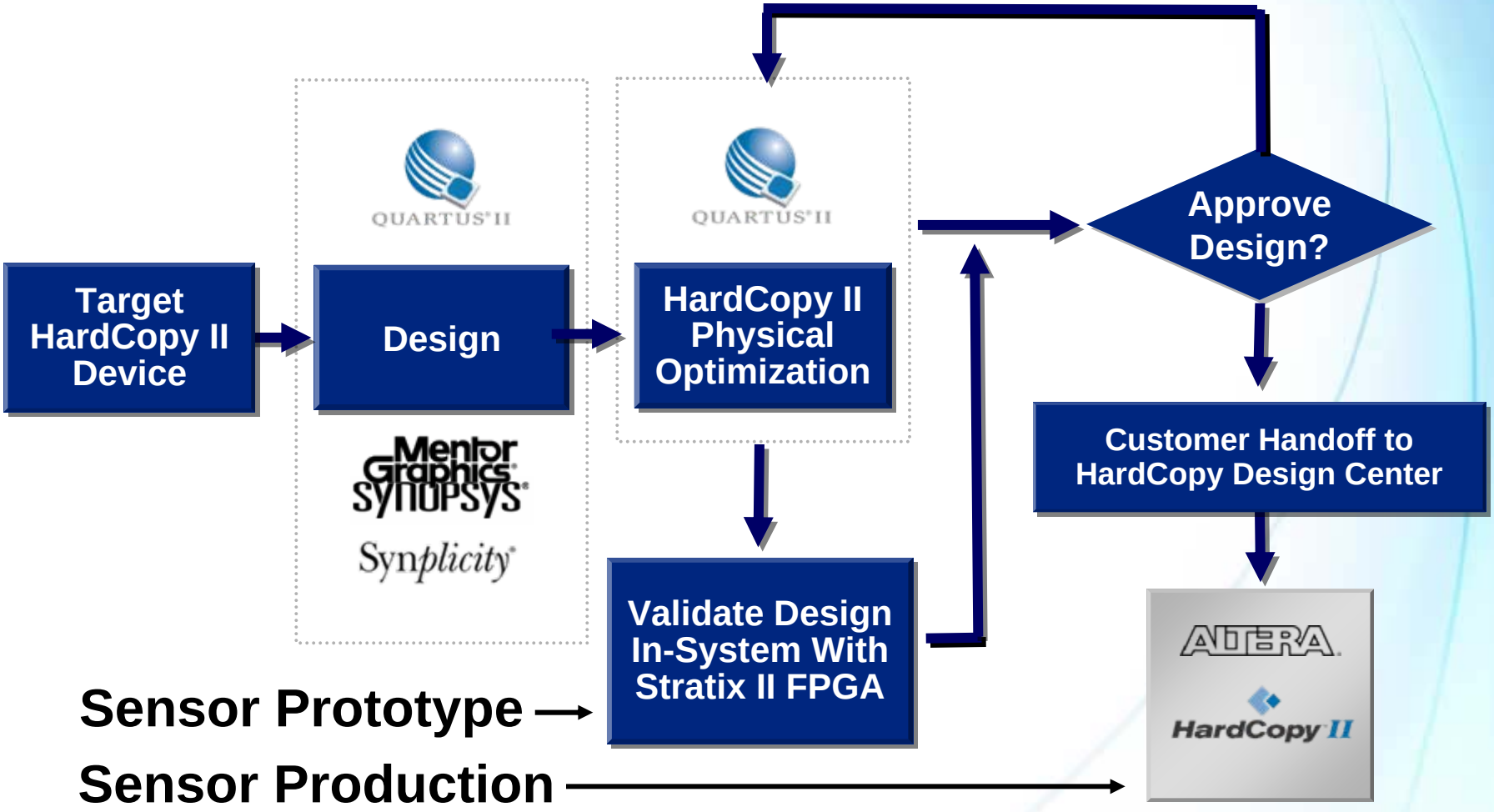
J Ryan Kenny
Jeff Wills
Altera Corporation
101 Innovation Drive
San Jose, CA 95134

Rick Pancoast
Ellis Taliaferro
Lockheed Martin MS2
199 Borton Landing Road
Moorestown, NJ 08057

High Performance Embedded Computing Workshop

18-20 September 2007

FPGA to HardCopy ASIC Device Design Flow



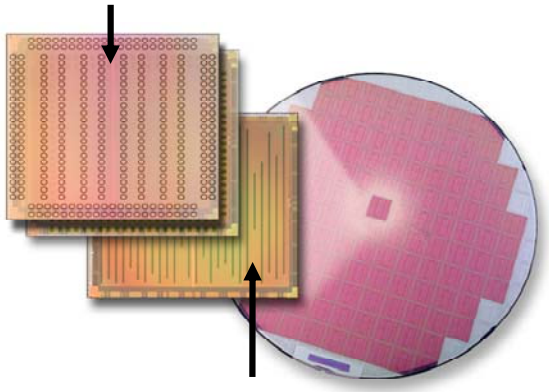
LOCKHEED MARTIN

ALTERA

Hard Copy ASIC Device – What

- True Structured ASIC
  - Only Top Layers Custom
- FPGA Architecture with ASIC Routing

Structured ASIC:
Customization Through Top Layers



Base Layer

Why

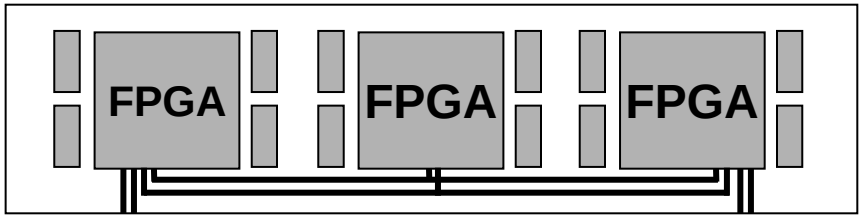
- Flexibility of FPGA Design with Cost and SWaP Features of ASIC
- Reduce:
  - Power by 50-70% (over FPGA)
  - Design time from 52 Weeks (ASIC) to 20 Weeks (Hard Copy)
  - Unit Cost after NRE estimated of $350,000
  - Risk – virtually zero risk conversion
  - Size by 60-85%
- Can be same pinout
- Up to 50% Performance Improvement

LOCKHEED MARTIN

ALTERA

Compute Node

(Notional Architecture)

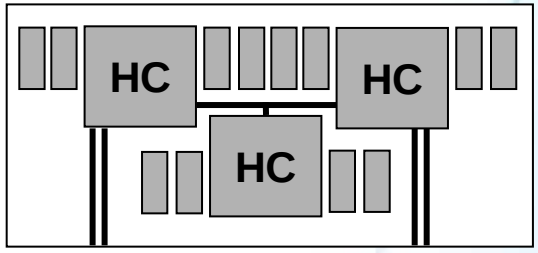


FPGA Compute Node (200 Watts)

Power:

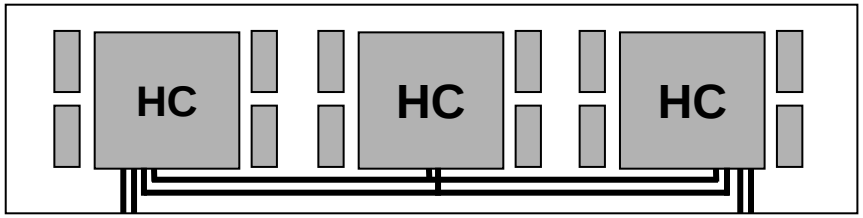
3 FPGA =	**60 Watts**
Memory\Other =	**40 Watts**
DC-to-DC Loss =	**20 Watts**
I\O (Serial) =	**80 Watts**

Create Smaller Module



Reduce Power by 80 Watts (40%)

Create Hard Copy Drop-In Chips



Reduce Power by 40 Watts (20%)

LOCKHEED MARTIN

ALTERA