Prototyping Advanced Military Sensor Systems Using FPGA-to-ASIC Design Flow

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Overview

Radar receiver design is seeing an increase in the number of digital tuning and digital signal processing (DSP) functions moved from processing single-board computers into fixed hardware logic. This results in two rising design challenges for digital design engineers: prototyping and testing highly sophisticated receivers, and designing for limited budgets for both power and heat dissipation.

An efficient FPGA-to-ASIC design flow transition provides solutions to both of these problems. The flexibility and prototyping advantages of the FPGA families allow all of the advantages of embedded systems programmability, while the transference of FPGA design to a structured ASIC allows for increased performance with reduced power and a reduced size footprint.

While the advantages of making this transition from FPGA to structured ASIC for production are well known, the cost and risk of making this transition are the deciding factors for engineering managers. Once these costs are both predictable and low, sensor board designers are likely to make FPGA-versus-ASIC decisions part of their standard design flow.

Prototyping Radar Systems

The National Missile Defense Ground Based Radar Prototype (NMD-GBR-P) is an example of a long-lead radar prototype program [1]. The NMD-GBR-P was designed to prove out active and passive array technology for missile defense. This program also sought to test and develop the intricate integrated activities of tracking, C4I, and battle damage assessment of a missile defense system, as well as system risk reduction.

From FY96-04, over $200 million was spent on the radar prototype alone. The Raytheon X-Band radar for Ballistic Missile Defense is expected to cost well over $1 billion, necessitating heavy prototyping for technology proving, sustainable engineering, and integration.

Distributed sensor systems, and radar data fusion, are other areas where prototyping and iterative design changes are essential. These applications driving more sophisticated modeling systems, and are well suited to FPGA and “blue board” prototypes. These early prototypes also help software developers innovate with better algorithms and tactics for best-fit detection and tracking. As an additional benefit, prototypes allow designers to examine architectural improvements to increase the maintainability of the system for increased design life.

Early prototyping and technology assessment is no longer the domain of just large systems developers. Even small radar and sensor systems are composed of multiple radiating elements and often-complex fast Fourier transforms for beam forming. After the significant cost and effort in proving out a system, faster paths from prototype to production are needed.

The role of the researchers and laboratories has become prominent in radar systems, and they have a greater set of responsibilities in making systems sustainable, testable, and fieldable.

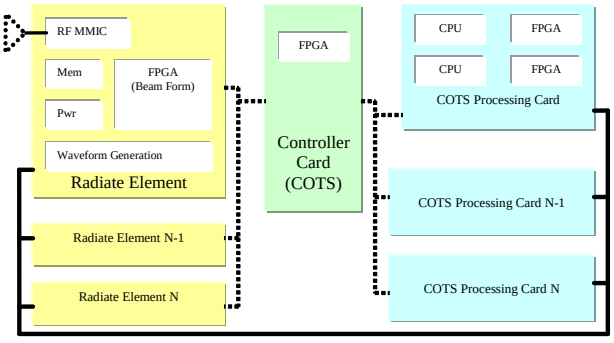

Figure 1: Representative Prototype RADAR System

Transition From FPGA to ASIC for Production RADAR Systems

Traditionally, the design trade-off in an engineering design between FPGA and ASIC was made on the basis of cost, development time, and risk. Designing “hard” chips is time-consuming, expensive, and errors often lead to expensive remanufacturing. FPGAs

reduce this design risk, though that comes with larger chip size, less power efficiency, and lower performance.

Miniaturization and cooling challenges are making size and power into critical design parameters. Therefore, the cost-versus-benefit trade of migrating a prototype design from FPGA to ASIC should be made.

A sample trade is made below using the design transition path from Altera® Stratix® III FPGAs to future HardCopy® structured ASICs.

It is important to note that the decision to pursue the receiver electronics design in an FPGA flow does not require any *a priori* design constraints for the FPGA designer. The decision to transfer to ASIC design can be made well into pre-production, after all prototyping, proof-of-concept, and algorithmic testing is performed using the FPGA design and test bench.

FPGA Architecture With ASIC Routing

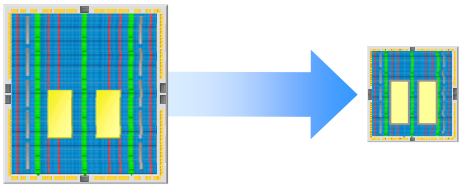

Figure 2: HardCopy Die Change (Stratix III FPGA to HardCopy Device)

Table 1: Summary of ASIC Benefits Over FPGAs

	HardCopy Structured ASIC
Power Improvement	Up to 70% less power (heat)
Size Improvement	65–80% smaller die
Performance Improvement	Up to 50% faster
Cost:	
Development Time	12–20 weeks (15–20% normal ASIC design)
NRE Cost	30% ASIC development cost or lower
Risk	Low hardware risk, virtually no algorithm risk
Flexibility	Low flexibility (compared to FPGA)

The transition from FPGA to ASIC allows the system design to become more compact, as the FPGA footprint and cooling requirements are reduced. However, the transition does not require a receiver board respin, as the HardCopy ASIC can be designed as a pin-for-pin replacement for the FPGA in the same package.

Additional advantages of ASIC implementation in advanced sensor systems include immunity to single event upsets (SEUs) and improved military-temperature performance. ASIC implementation sometimes requires additional compliance with International Trade in Arms Regulations (ITAR), which the HardCopy Design Center offers.

HardCopy Design Flow

The design transfer from FPGA to ASIC for the HardCopy family is shown below. This demonstrates the significant advantages of the FPGA-to-ASIC design flow over developing a new integrated circuit.

The same code synthesis can be used for both the FPGA and structured ASIC design. The Altera Quartus® II design tools then allow the designer to perform separate physical optimizations for a targeted FPGA and an ASIC die. This results in two different netlists, which can be used for either FPGA implementation or ASIC design performed at a HardCopy Design Center. A receiver design can progress through several prototype versions within a radar test bed before returning to the synthesis step and pursuing a HardCopy device.

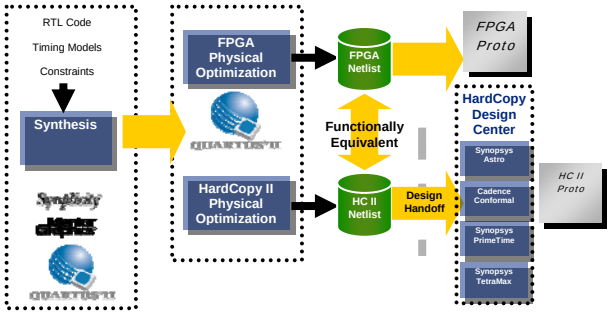

Figure 3: HardCopy Design Flow

Summary

With the increasing digital complexity of radar system design, engineers should maintain as much flexibility as possible through system definition and prototyping with respect to digital logic elements. Later, when system manufacturing and production systems are made, the program manager still has several options to meet changing requirements on cost, power, heat, performance, and form factor. FPGA's have long offered maximum design flexibility, and the design transition option to structured ASIC increases that flexibility for radar system designers. Preparing a solid design architecture path that allows (but does not

require) a structured ASIC transition ensures that flexibility.

References

[1] *National Missile Defense RDT&E Budget Justification Sheet.* Federation of American Scientists (FAS), March 1996. http://www.fas.org/spp/starwars/budget/peds_97/603871c1.htm