SmartCell: A Coarse-Grained Reconfigurable Architecture for High Performance and Low Power Embedded Computing

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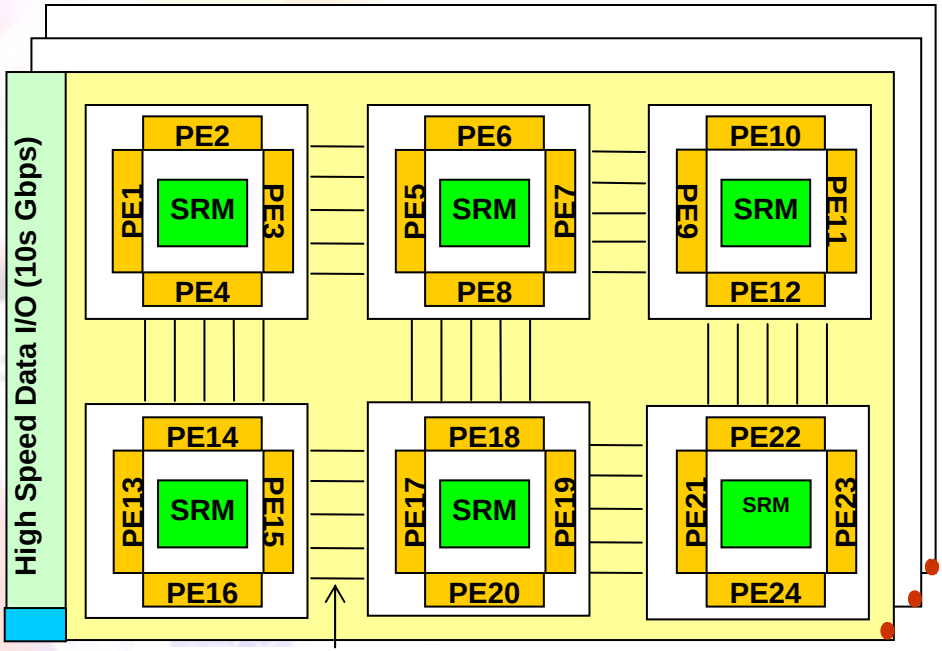
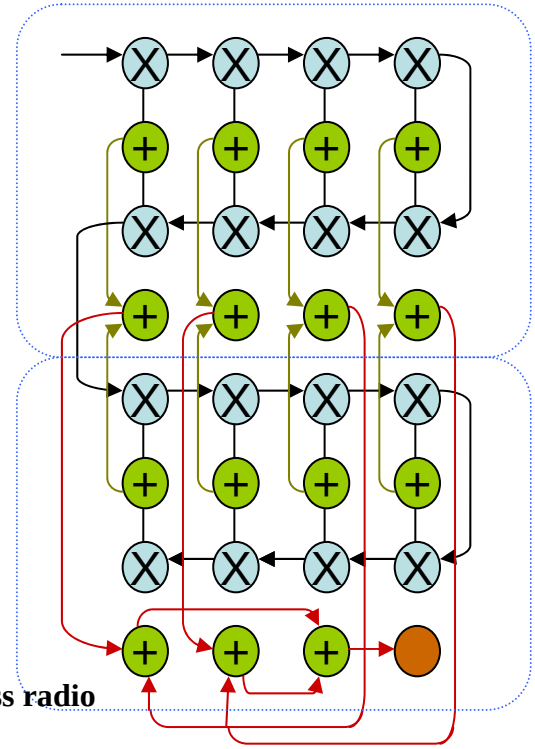
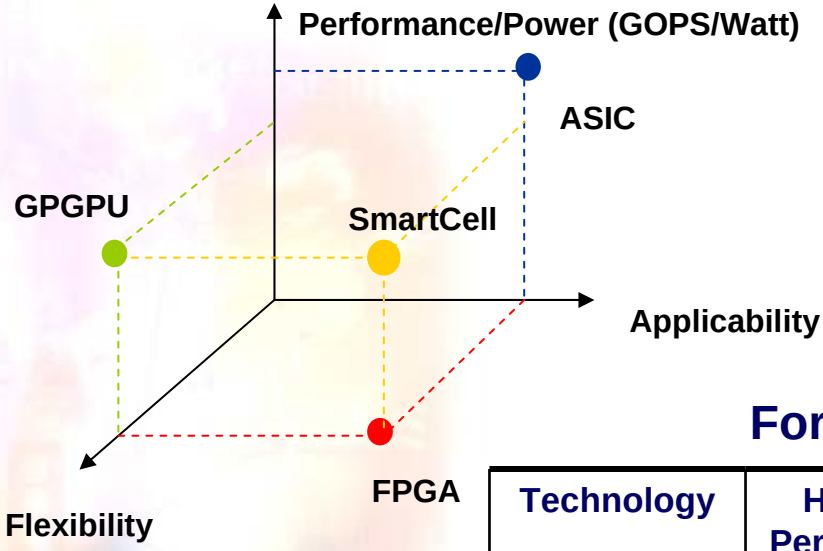
Architecture overview

- **Thousands of pico-processors interconnected with high-speed switching fabrics within a single chip**
  - **Goal: low-power, high-performance, reconfigurable, and applicable**





Performance Metrics, Technical Challenges, and Applications



Technical Challenges:
- Low power core functions
- Interconnections (wiring and routing)
- Compiler (hardware/alg co-design)
- Reliability (evolvable algorithms)

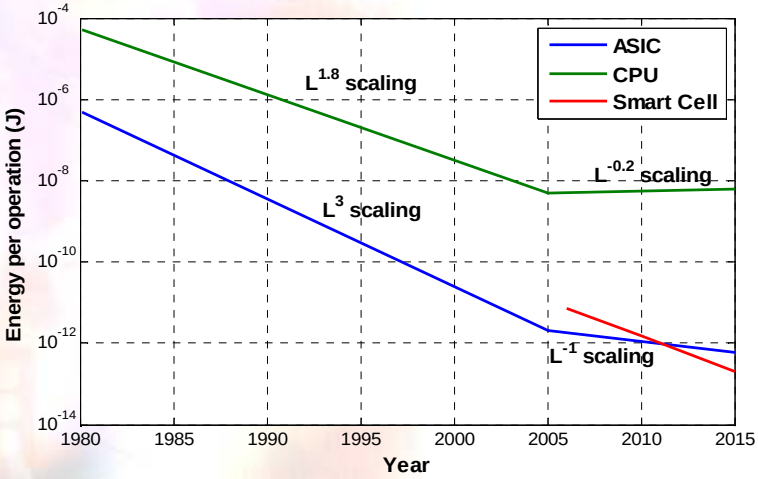
Target Performance:
- 1,024 ALU core
- 100 MHz
- 500 mW
- 200 GOPS

For Defense and Space Applications

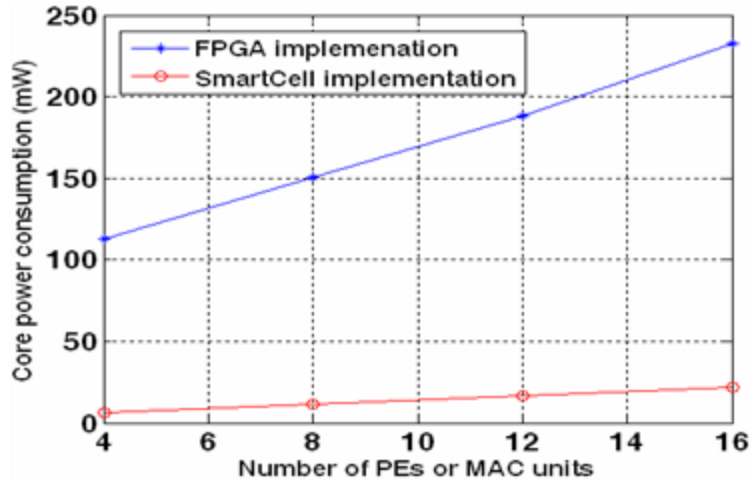
Technology	High Perform-ance	Low Power	Program-mable	Applic-able	Evolvable (Self-healing)
FPGA	Y	N	Y	Y	Y
CPU/DSP	N	N	Y	Y	N
GPU	Y	N	Y	N	N
ASIC	Y	Y	N	Y	N
SmartCell	Y	Y	Y	Y	Y

Experimental Performance

Energy efficiency perspectives



Benchmark performance of FIR filters



Performances of fully pipelined 16-tap FIR filter

	Dynamic Power	Core Power	Gate equivalent
Smart-Cell	20.3 mW	21.7 mW	265 k
FPGA	157.6 mW	232.6 mW	82 k

2 by 2 SmartCell implementation:

- TSMC 130 nm ASIC library;
- 1.33 mm²;
- >500 MHz operating freq.;
- 10~18 times more power efficient than FPGA implementations;