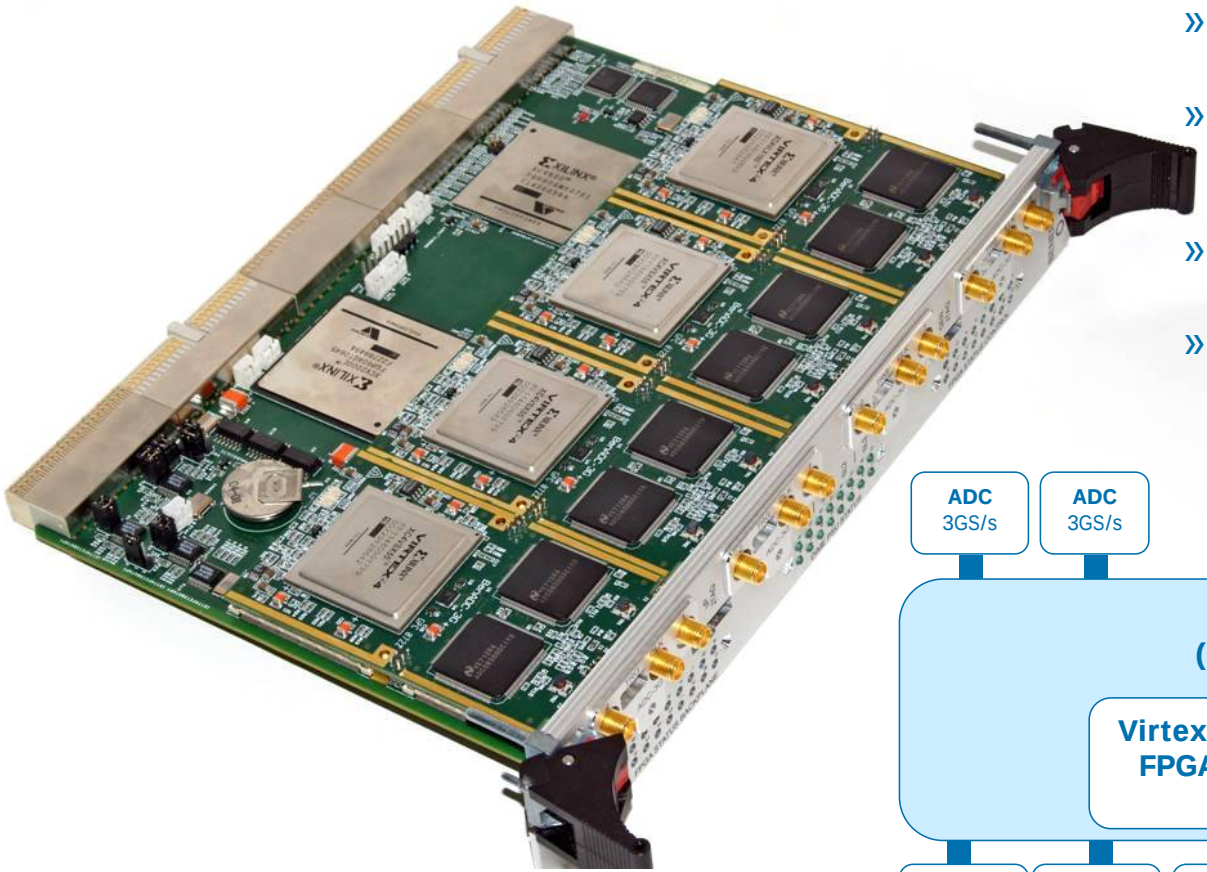
A Streaming FFT on 3GSPS ADC Data using Core Libraries and DIME-C

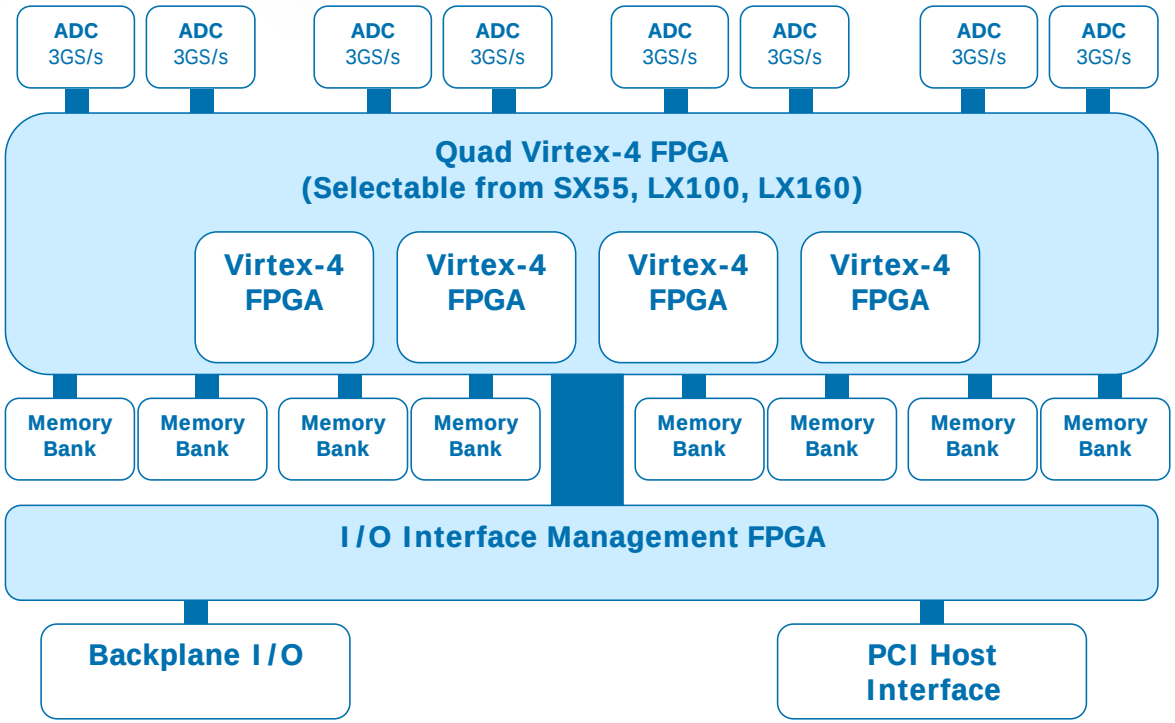
Malachy Devlin, CTO, Nallatech
Robin Bruce, EngD Research Engineer, ISLI
Chee Kin Tang, MSc Student, ISLI
www.nallatech.com

Nallatech
Our Expertise. Your Success.

Reconfigurable Computing Platform

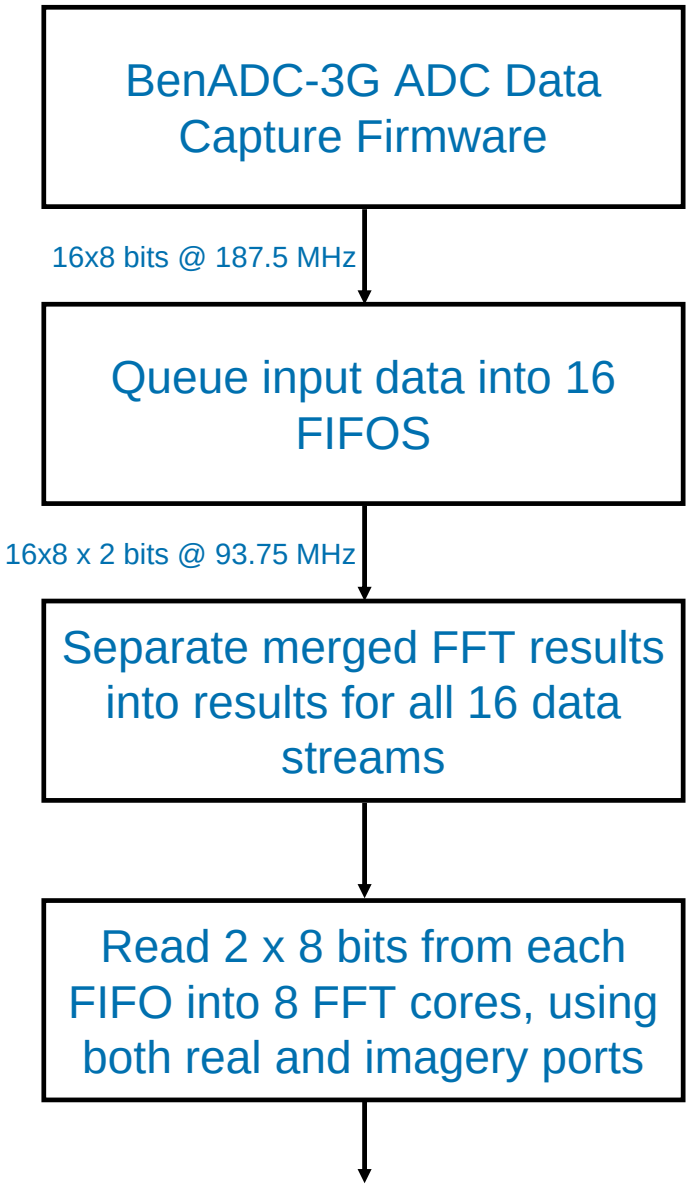


- Multi Channel Acquisition System
  - Scalable from 2 – 8 channels
- Dual Channel 3GSPS 8-bit ADC Modules
  - Uses 2 National Semiconductor ADC083000
  - Dual Channels for I/Q Applications
- Xilinx Virtex-4 FPGA
  - LX100, LX160, SX55
- 64Mbytes DDR-II SRAM



Nallatech
Our Expertise. Your Success.

System Design for 3GSPS Pipelined FFTs



- **Hardware Efficient FFT Algorithm**
  - FFT Core has Real and Imaginary Inputs
  - Only transforming real data, hence compute two real streams using single FFT core
  - Theory as follows:
- Assume that F(n) is the fourier transform of f(n), where n ranges 0 to N-1 with N the transform size.

$$f(n) = a(n) + j \times b(n)$$

$$F(n) = X(n) + j \times Y(n)$$

- if we set a(n) = f1(n) and b(n) = f2(n) where f1 and f2 are two independent real functions in the time domain, we can obtain their transforms as follows:

$$F_1(n) = X_{even}(n) + j \times Y_{odd}(n)$$

$$F_2(n) = Y_{even}(n) + j \times X_{odd}(n)$$

- where

$$X_{even} = (X(n) + X(N-1-n))/2$$

$$X_{odd} = -1(X(n) - X(N-1-n))/2$$

Nallatech
Our Expertise. Your Success.

DIME-C & Core Libraries

- DIME-C presents user with a software-like development environment
  - Uses a Subset of ANSI C Syntax
  - Handles ANSI C Datatypes
  - Plus boolean and FIFO types
- Compiles Input C code to VHDL and pre-synthesized logical netlists
- Leverages pre-existing hand-coded IP cores, either:
  - Natively, as in the case of basic arithmetic operations, or
  - Via the inclusion of libraries of IP cores
    - Analogous to software function calls
- Core Libraries consist of three elements:
  - .h header file, for function call prototypes
  - .lib file, XML file that carries metadata regarding the cores, e.g. datatypes of ports, latency, clocking, port naming, support files etc…
  - Support Files
    - Raw HDL, EDIF, NGC, etc.
- OpenFPGA CORELIB Working Group
  - Industry and Academia working towards defining a single standard for Core Libraries in FPGA high-level languages
  - Aim is to promote the migration of IP to and between FPGA High-Level Compilers

Nallatech
Our Expertise. Your Success.