Evaluating Partial Reconfiguration for Embedded FPGA Applications

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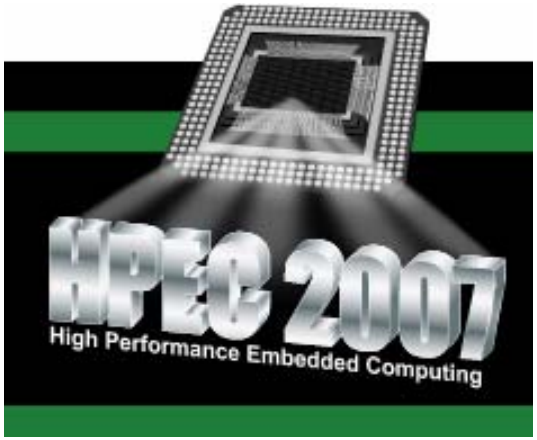

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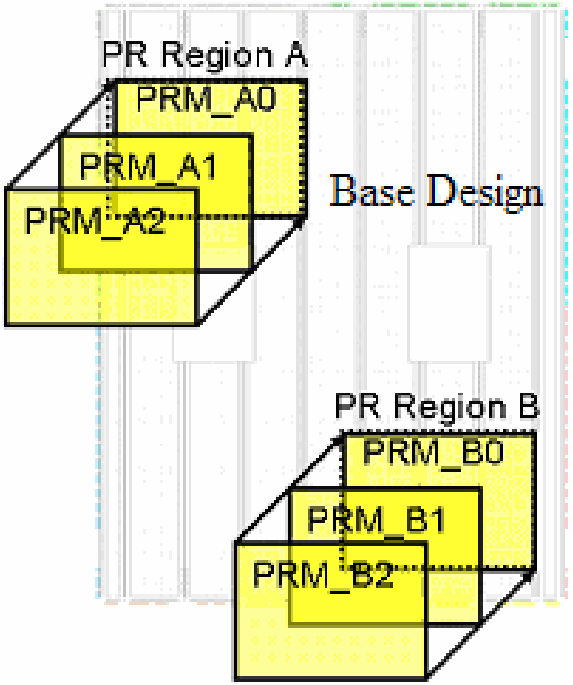
Partial Reconfiguration

- Partial reconfiguration (PR) has existed throughout the history of Xilinx's Virtex FPGA family
- Commercial interest in PR has never materialized due to a lack of supporting software tools and a merciless design flow
- Recent changes however:
  - Release of Virtex-4 and Virtex-5 series with tile-based configuration architectures
  - Lucrative software-defined radio (SDR) market => new mainstream design flow supported by Xilinx
- However, relatively recent and still restricted release of this new design flow has left a vacuum in research and results exploring PR systems targeting these new devices
- First question that needs to be answered:
  - What is performance impact of this new flow when targeting Virtex-4 FPGAs?



Partial Reconfiguration

- Platform for analysis: Remote Updating
- Is there a way to maintain true field reprogrammability in deployed systems using partial reconfiguration?
  - In-Application Programming for RC
  - Dynamically tailor hardware to application's needs in real-time
  - Prevent embedded FPGAs from becoming expensive, low-performance, power-hungry ASICs
  - Minimize need for external hardware through PR
- Various high-performance computing cores used to evaluate system performance
  - Radix-4 FFT
  - AES
  - ARM7 soft-core
- Metrics include:
  - Clock Frequency
  - Bitstream Size
  - Resource Overhead