Evaluating Partial Reconfiguration for Embedded FPGA Applications

CHREC NSF Center for High-Performance Reconfigurable Computing

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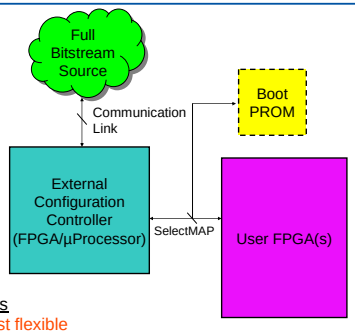
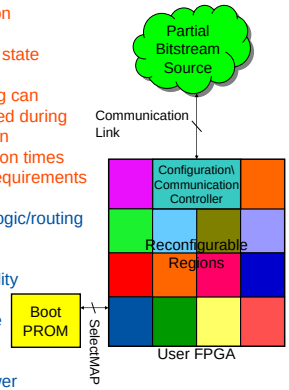
Baseline

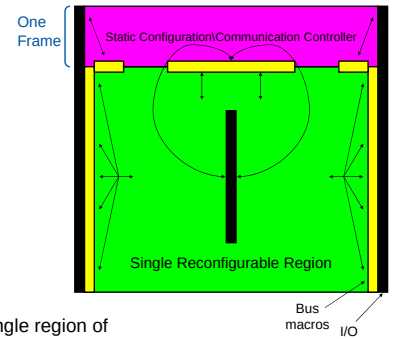


- Pros
  - Most flexible
  - Simplest module development with highest performance
  - Configuration controller can be radiation-hardened
  - 100% of user FPGA logic/routing resources available
- Cons
  - Highest communication bandwidth
  - State information not maintained
  - Longest reconfiguration time
  - SelectMAP pins usually no longer usable as general purpose I/O
  - Higher power/PCB requirements
  - More points of failure

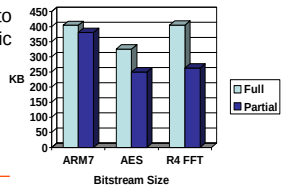
- Pros
  - Lower communication bandwidth
  - Possible to maintain state information
  - Unrelated processing can continue uninterrupted during partial reconfiguration
  - Shorter reconfiguration times
  - Lower power/PCB requirements
- Cons
  - Less than 100% of logic/routing resources available
  - High overhead
  - Radiation susceptibility if COTS
  - More difficult module development
  - Varying degrees of flexibility (always lower than non-PR baseline)



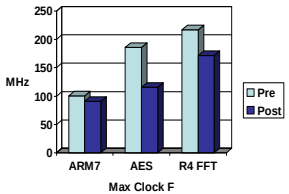
Architecture #1



- 1 single region of maximal size
- Has exclusive access to all I/O not used by static region
- I/O type is reconfigurable

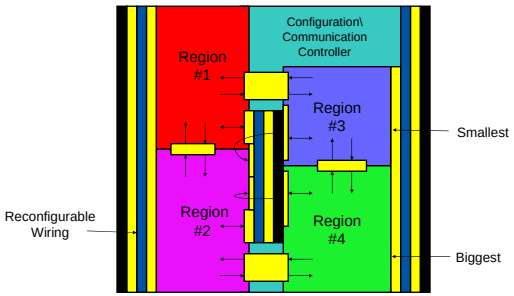


- Pros
  - Conceptually simplest – only one PRR
  - Lowest overhead
  - Least performance degradation
  - Easiest development framework
- Cons
  - No maintenance of state information
  - Highest PR bandwidth
  - Least amenable to current Xilinx toolset



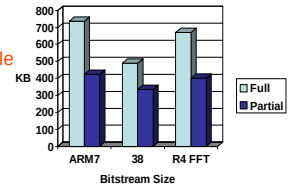
	Slice Usage	XC4VLX25 Utilization
Reconfigurable Region	8320	77.4%
Static Controller	1910	17.8%
Bus Macro Overhead	522	4.9%

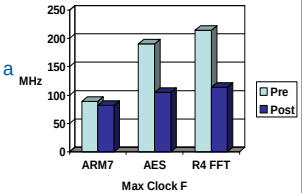
Architecture #2



- 4 Regions of varying size

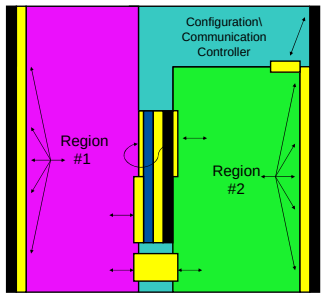
- Pros
  - Maintenance of module state information
  - Lowest PR bandwidth
  - More amenable to current Xilinx toolset
- Cons
  - Conceptually most difficult – 7 PRRs
  - Must partition I/O and communication using a best guess at design-time
  - Highest overhead
  - Most performance degradation



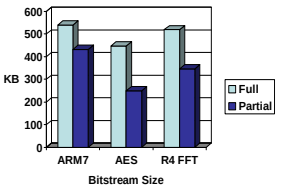


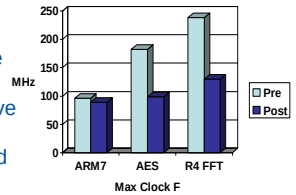
	Slice Usage	XC4VLX25 Utilization
Region 1	1536	14.3%
Region 2	1536	14.3%
Region 3	1408	13.1%
Region 4	2112	19.6%
Static Controller	1784	16.6%
Bus Macro Overhead	1508	14.0%
Wiring	868	8.1%

Architecture #3



- Meet in the middle
- Attempts to offer a balance between the pros and cons of #1 and #2
  - 2 Regions
  - Left I/O exclusive to #1
  - Right I/O exclusive to #2
  - Middle I/O shared





	Slice Usage	XC4VLX25 Utilization
Region 1	3840	35.7%
Region 2	4160	38.7%
Static Controller	1664	15.5%
Bus Macro Overhead	792	7.4%
Wiring	296	2.8%