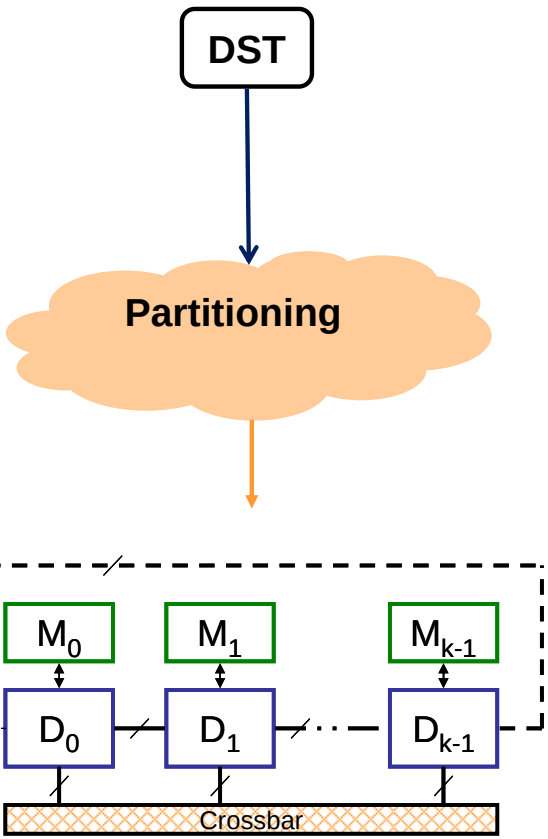
MOTIVATION AND OBJECTIVE

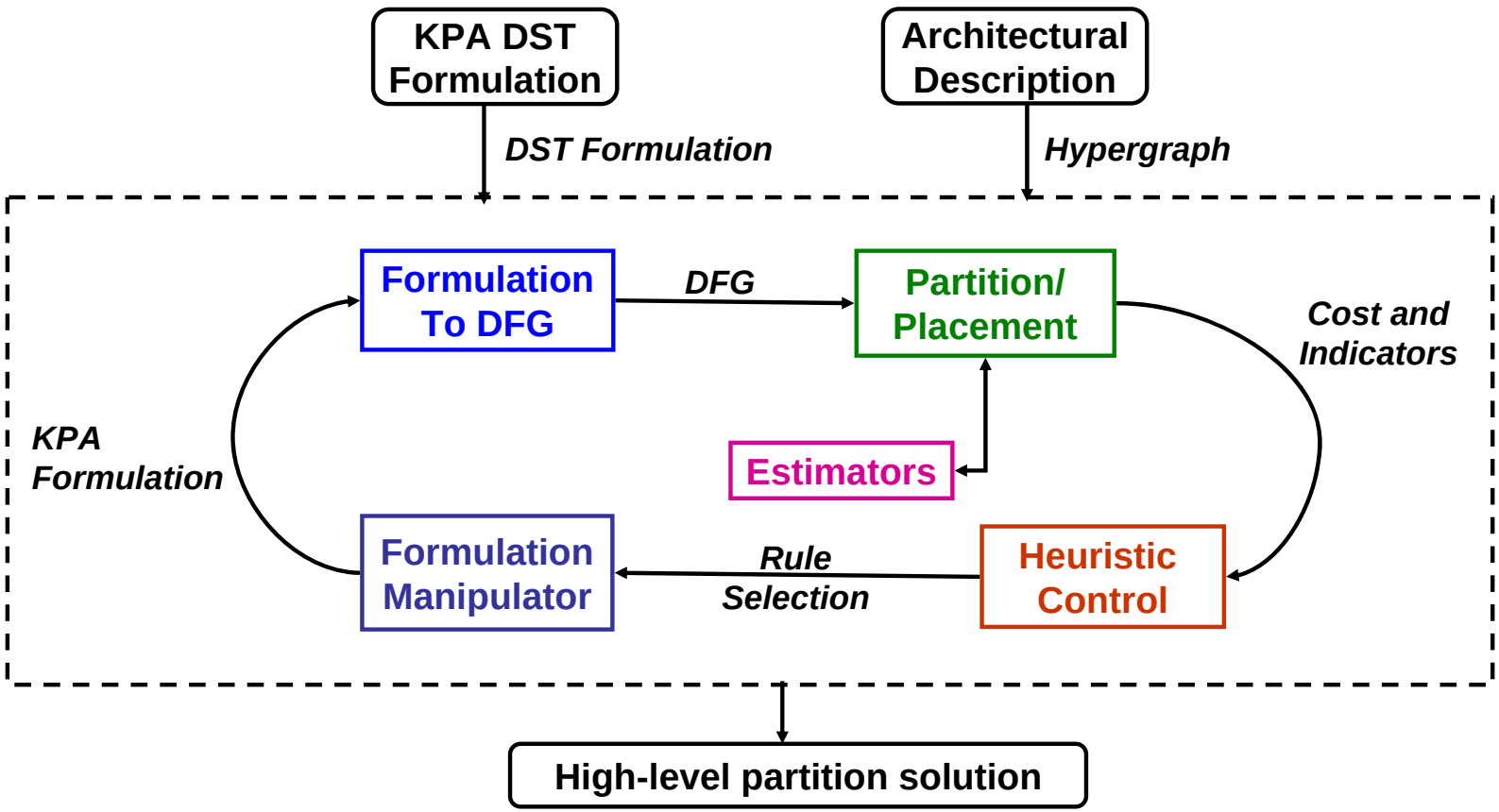
- **Discrete Signal Transforms (DSTs)**
  - DFT, DCT: major performance component in many applications
  - Hardware accelerated but at high area cost
  - Example: 4P DFT formulation and others
- **Distributed (dedicated) hardware architectures (DHAs)**
  - Partitioning plays key role in performance and resource optimization.
- **Partitioning beyond multi-device**
  - Multi-core GPPs: IBM CELL BE, Intel Core Duo
  - System-on-Chip: Network-On-Chip
- **Need tools to aid in partition exploration, mapping, implementation → design automation**
- **Can we improve partitioning by introducing high-level DST considerations?**



Distributed Hardware Architecture

DMAGIC METHODOLOGY

DMAGIC = DST Mapping using Algorithmic and Graph Interaction and Computation

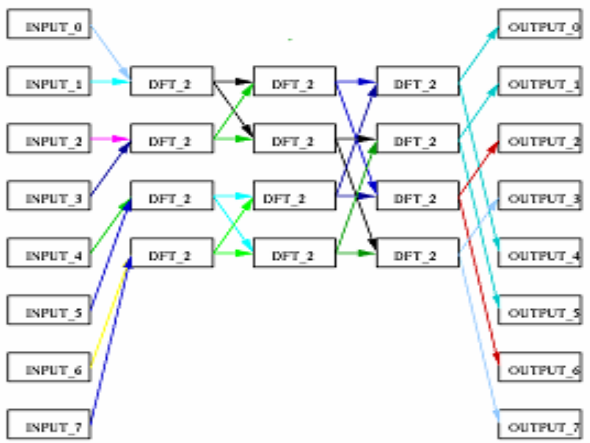


TOOLS

Kronecker to Graph Tool

$$(F_2 \otimes I_4)(I_2 \otimes F_2 \otimes I_2)....$$

KTG



Weighted DFG with level information

Operator matrices: Identity, Transform, Permutation, Unitary, Unitary Transpose, Twiddle

KPA operations: Tensor product (⊗), Direct Sum (⊕), Matrix Multiplication

Graph partitioning/placement algorithm

- P/P inspired by Kernighan Lin bipartition heuristic
- Extended to k-way partitioning for heterogeneous channels
- Cost function sensible to DHA main concerns
- DST graphical considerations heuristics

Cost Function

$$P = \langle \Phi_0, \Phi_1, \ldots, \Phi_{m-1} \rangle$$

$$\Phi_i = R_i \times W_i$$

W_i → *weight of channel i*

R_i → *required comm. through i*

FORMULATION EXPLORATION

Objective: Use DST rules to explore space of equivalent formulations in search for one that better suits the target architecture.

Challenges: Combinatorial explosion of the solution space.
Find rules amenable to hardware implementation.

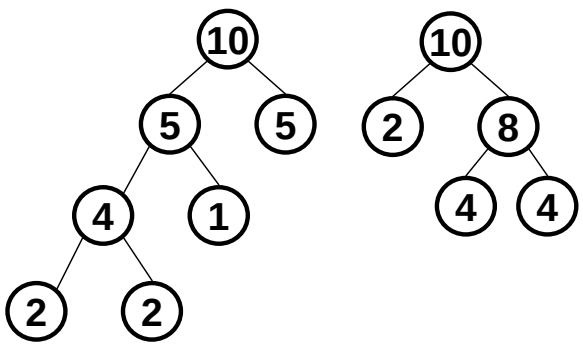
Approach: Conducted experiments to assess the impact of transformations on partition quality.
Results used to devise exploration strategy.

Experiments:

Effect of inter-column permutations
Effect of node granularity

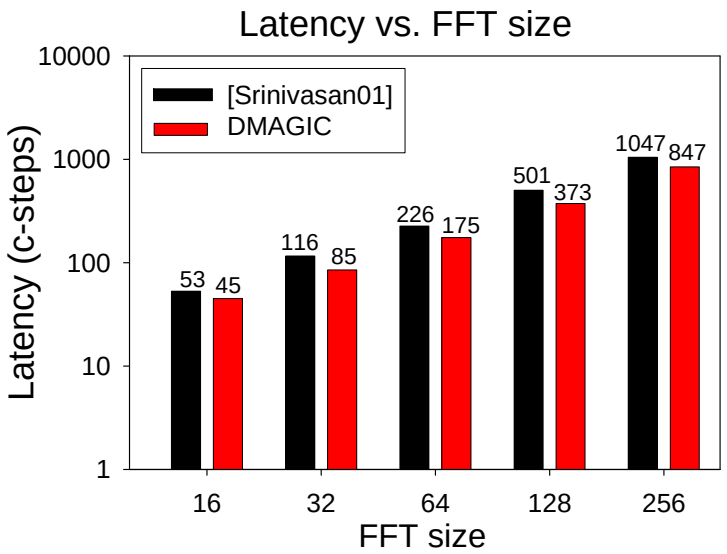
→ *Have effect on solution quality, yet hard to establish heuristic.*

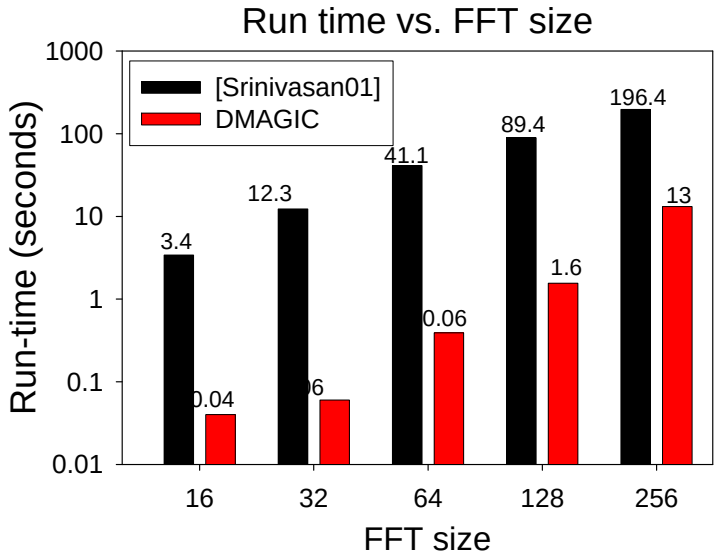
Effect of breakdown strategy using DST decomposition rule

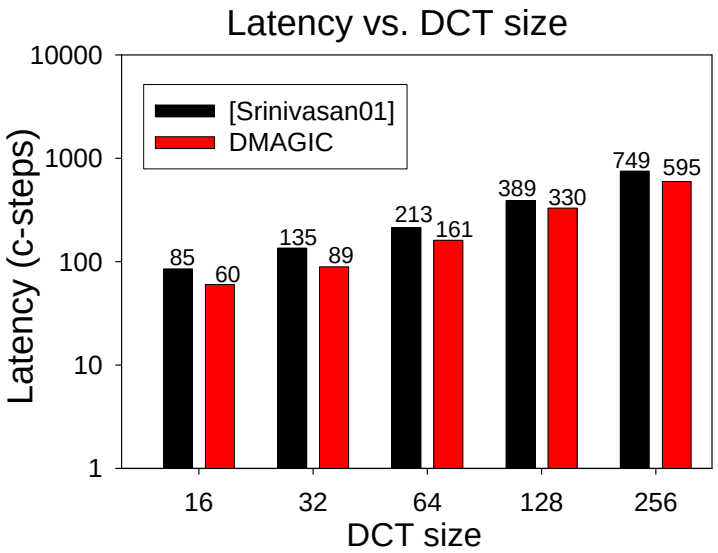


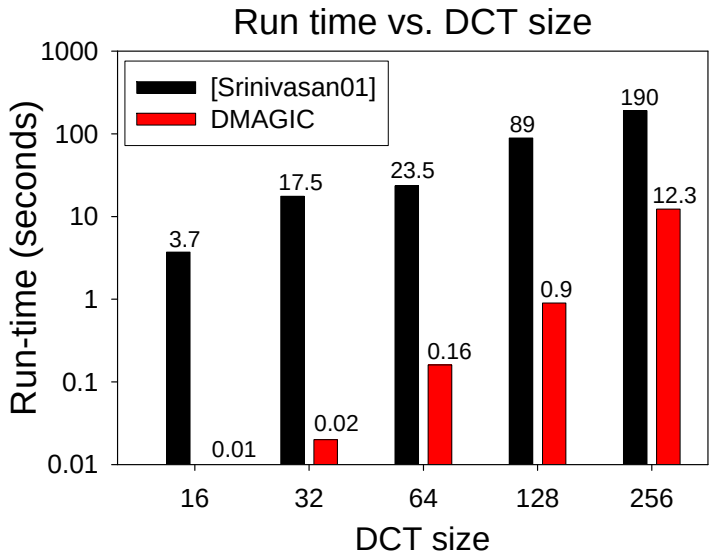
Observations on exhaustive small sized transforms → Greedy ‘top-down’ formulation exploration using breakdown strategy

RESULTS









- **Latency Reduction: Average = 23.3%, Peak = 34.1%**
- **Run-Time Reduction: Average = 98.0%, Peak = 99.9%**

CONCLUSIONS AND CONTRIBUTIONS

- **Multiple opportunities to improve partitioning by taking advantage of DST and DHA features.**
  - **Graph level: regularity of permutations and operations.**
    - **Graph partitioning and area estimator can be made more sensible to DHA and DST concerns**
  - **Algorithmic level**
    - **Reformulation has significant impact on partition quality**
    - **Improvements over generic methodology**
- **Latency reduction (23.3% avg, 34.1% max), Runtime (98.8% avg, 99.9% max)**
- **Tools:**
  - **KTG: automated and extensible methodology for conversion of Kronecker product algebra (KPA) formulations into DFGs**
  - **Architectural model and high-level estimator for the implementation of distributed DSTs**
  - **Graph partitioning heuristic for k-way for DSTs to DHAs**
- **New heuristic for exploring DST formulation space**
- **New arbitrary decomposition DCT formulation**