World's First Polymorphic Computer -- MONARCH

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MONARCH Processor Status

MONARCH, the world's first polymorphic computer is here. Functional sample chips are in the lab and being used to run software and perform demonstrations. Our presentation will begin with an overview of the key concepts and features of MONARCH. We will then discuss the methodology and status of MONARCH characterization and benchmarking. Results to be discussed include measurements of processing throughput, I/O capacity, and power efficiency. We will close with a discussion of future directions for the use of MONARCH as an innovative system enabler.

MONARCH Features

The MONARCH (MOrphable Networked micro-ARCHitecture) chip, which can adopt different forms depending on processing objectives, is arguably the most power-efficient processor available today. A typical processor is optimized for either front-end signal processing or back-end control and data processing. The MONARCH processor is unique in its ability to reconfigure itself to optimize processing on the fly. MONARCH provides exceptional compute capacity and highly flexible data bandwidth capability coupled with state-of-the-art power efficiency and full programmability. MONARCH is also a scalable architecture ranging from single chip solutions for highly embedded systems, to arrays of chips for teraflop throughput.

MONARCH was developed to address the future requirements of advanced military and commercial systems, and to significantly improve the processing throughput and efficiency of high data input/output systems. In the commercial environment, this will have tremendous utility in embedded, power-constrained computing applications, while military technology could foreseeably make a leap to the next generation of high-tech systems, including modern Radar, E/O, Missile, Communications, and SIGINT systems. It permits the development of systems that require very small size, low power, and in some cases radiation tolerance. Key attributes that differentiate MONARCH include:

- The ability to handle multiple computing models: Multiple Instruction Multiple Data (MIMD), Single Instruction Multiple Data (SIMD), and Streaming
- Distributed inter-node communication provides exceptional on-chip bandwidth
- Reconfigurable computational array (FPCA), which provides ASIC like performance with microprocessor-like programmability
- A distributed processor architecture making the chip highly scalable and fault tolerant
- System-on-a-chip (SOC) computing minimizes cost and area associated with peripheral components and improves power and volume efficiency (GFLOPS/Watt; GFLOPS/m3)

MONARCH Architecture

Each MONARCH chip contains six RISC processors and a reconfigurable computing array containing 96 processing elements (32-bit integer and IEEE floating point). The external interfaces include two DDR2 memory interfaces for bulk data storage, two Serial RapidIO ports for command and control, a flash memory interface for booting and 16 high bandwidth serial links for inter-chip communication and sensor interface. The MONARCH processor can sustain 64 GFLOPS (giga-floating point operations per second) of throughput while consuming under 20 Watts. In addition, each chip also features more than 60 giga-bytes per second of memory bandwidth and more than 43 giga-bytes per second of off-chip data bandwidth.

The MONARCH architecture is shown in Figure 1. :

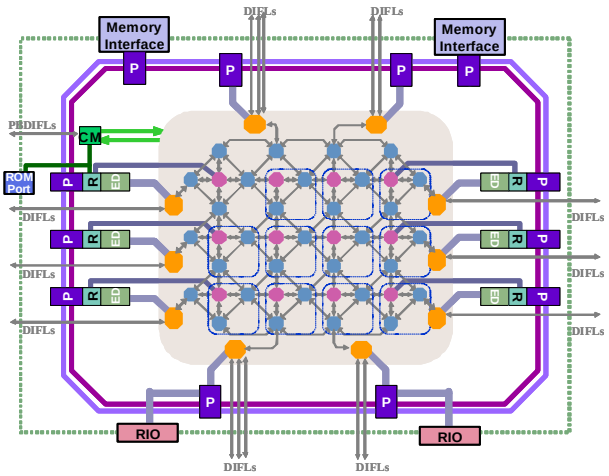

Figure 1: Monarch Chip Architecture.

The MONARCH chip has been developed under contract to DARPA IPTO (Defense Advanced Research Projects Agency Information Processing Technology Office) and under the auspices of their PCA Program administered by AFRL Wright Patterson. Raytheon was the prime contractor on the XMONARCH development, and was partnered with USC/ISI, Exogi, Mercury Computers, IBM and Georgia Tech for specific intellectual property. IBM fabricated the chip in their Cu08 (90nm) CMOS ASIC process.