



Spaceborne Processor Array in Multi-Functional Structure (SPAMS)

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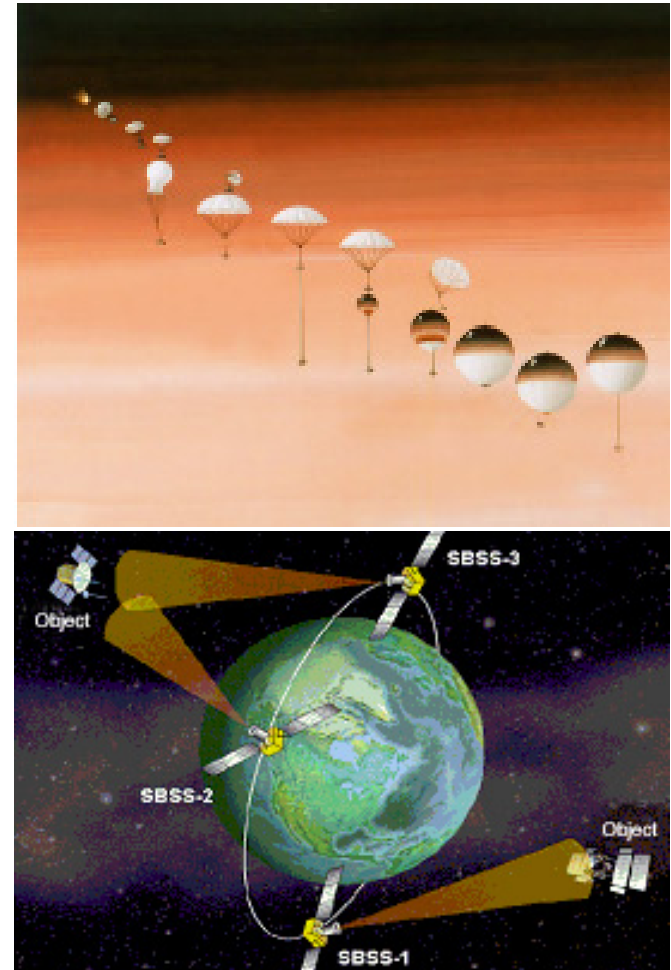
High Performance Embedded Computing (HPEC) Workshop

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Introduction

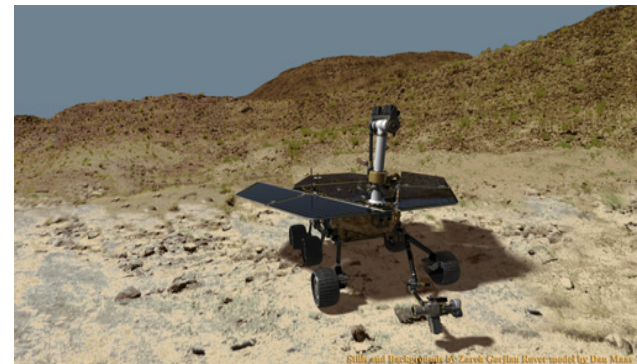
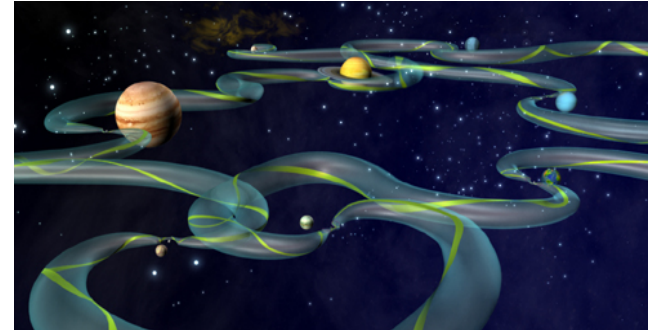
- **Future NASA missions require high performance on-board processing capability yet will be severely limited by mass.**
 - Autonomous Science
 - Constellation Control
 - Formation Flying
 - Virtual Presence
- **DoD space programs such as Space Superiority can also benefit from high performance on-board processing.**
 - Space Situational Awareness
 - Real-time Spacecraft Tracking
 - Autonomous Operations Under Interferences





Future Autonomous Mission Drivers

- **Interplanetary Navigation**
 - Low thrust in-orbit
 - Lagrange point
- **Entry Descent & Landing**
 - Flight control thru disparate flight regimes
 - Landing zone identification
 - Lateral winds
 - Soft touchdown
- **Surface Mobility**
 - Terrain traversal
 - Obstacle avoidance
 - Science Target identification
 - Exploration sequencing





Future Mission Requirements

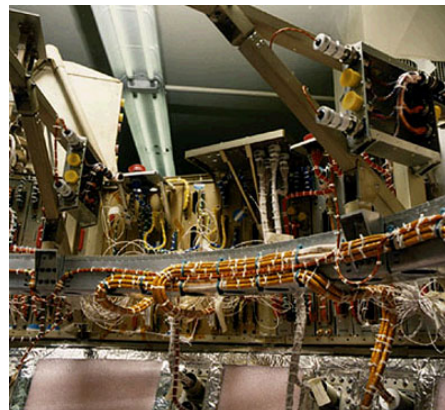
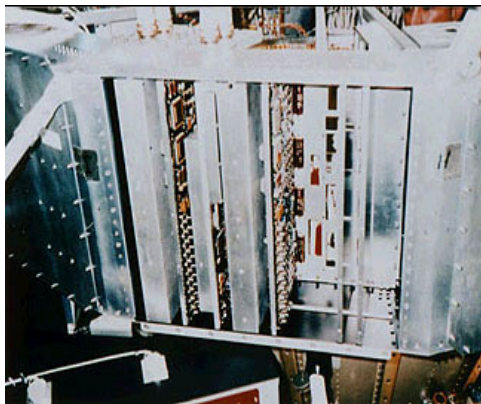
- **Teraflops' in space**
 - Satisfy wide range of mission drivers
- **Ultra low energy per operation**
 - Towards > 100 Gops/watt
- **Numeric and Symbolic high performance computing**
 - Numeric for remote sensor data analysis and knowledge extraction
 - Symbolic for real-time context-aware planning and goal-directed contingency response
- **Long duration fix-less operation**
 - Multi-decade
- **Size and weight**
 - Small enough to fit in constrained volume
 - Light enough to be applied to virtually all autonomous mission profiles and costs
- **Scalable**
 - Up to high performance in space
 - Down to smallest possible mission packages
 - Single software stack hierarchy and cognition model
 - High reliability software
 - Low software development time



Current Spacecraft Electronics



- Centrally Located Chassis and Backplanes.
- Aluminum or Titanium Based Structural Members.
- Heavy and Complicated Wiring Cables.
- High Performance Computers Often Sacrificed During Spacecraft Trade-off Analysis.

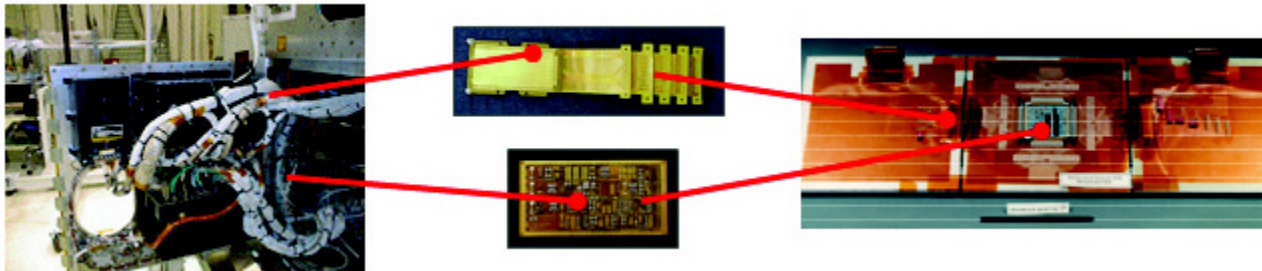




Multi-Functional Structure (MFS) Technologies



- **The NASA, AFRL, MDA, SMC, and DARPA have also been supporting the technology development of the MFS .**
 - NASA Deep Space-1, NASA EOS-1, Boeing Delta IV ELV, and Global Hawk UAV.
- **Spacecraft built with MFS can have:**
 - >50% mass reduction.
 - >2x volume saving.
 - Support mass production of spacecraft for constellations
- **Most MFS work focuses on embedding lightweight, flexible circuits into composite structures.**



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SPAMS Objectives

- **On-demand supercomputer level performance aboard spacecraft.**
- **High performance processing without increase to spacecraft mass.**
- **Dynamic ultra low power consumption.**
- **Long lifetime fault tolerance.**
- **High survivability in hostile environments.**



PC Board Material Property



Material	Thermal Conductivity (W/m*K)	CTE (ppm/C)	Density (g/cm³)	Tensile Modulus (msi)
ST325 [1]	325	-1.15	2.17	114.0
FR4 [1]	8.0	17.00	1.80	2.4
Polyimide [1,2]	0.3	16.50 X,Y dir	1.70	3.0
Copper [1]	385	17.00	8.92	12.0
Al 100%[1]	240	24.00	2.70	10.2

References

[1] Technology Overview, from Thermal Works website: <http://www.thermalworks.com/marketing/STABLCOR%20Properties%20Chart.pdf> accessed 4/20/06

[2] Internal JPL verbal communication- Results of TMA testing



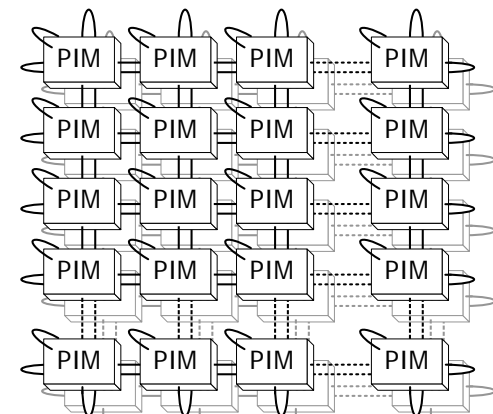
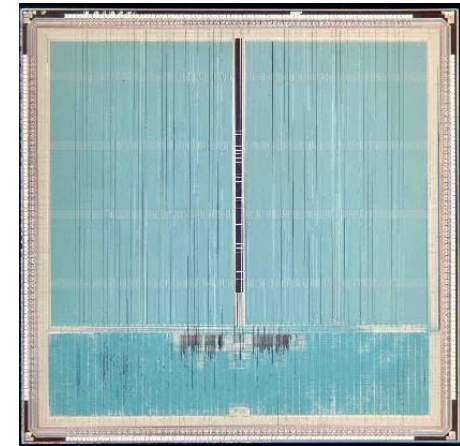
SPAMS Approach

- **Instead of embedding flexible circuits into composite structures, SPAMS takes advantage of the strength characteristics from the new composite materials and builds the spacecraft structure members with printed circuit boards.**
 - Direct Die Mounting on PC Boards.
 - Unlimited Expandability for Array Processors.
 - High Survivability.
- **Integrate with *Gilgamesh Memory, Intelligence, and Network Device (MIND)* multi-core in-memory computer architecture into a single, system super-architecture.**
 - Ultra High Performance
 - Ultra Low Power
 - Long Duration Fault Tolerance.



MIND Strategy

- **Multi-Core Memory**
 - Very low power
 - High memory bandwidth
 - Low memory access latency
 - Single system image for scalable computation
- **Graceful Degradation**
 - Exploits repetitive structures and redundant data paths
 - High reliability with no maintenance
 - Reconfiguration for fault isolation
- **Active Power management**
 - Decrease average power consumption
- **Real time processing**
 - Control of actuators and post sensor processing
- **Advanced execution model for efficient scalability**
 - Message driven-computing split-transaction
 - Multithreaded task control
 - Lightweight synchronization
 - Dynamic parallelism





MIND Architecture

- **Parcel active message driven computing**

- Decoupled split-transaction execution
- System wide latency hiding
- Move work to data instead of data to work

- **Multithreaded control**

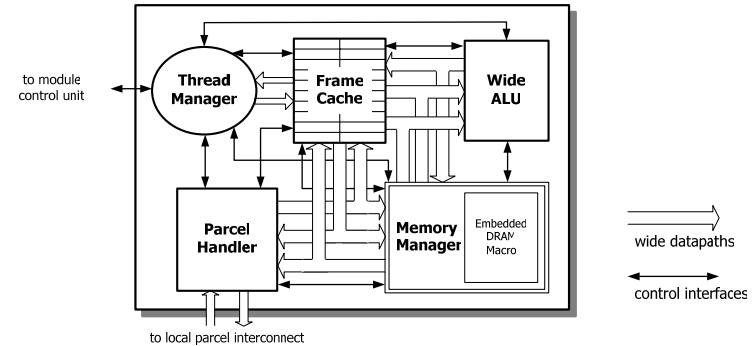
- Unified dynamic mechanism for resource management
- Latency hiding
- Real time response

- **Virtual to physical address translation in memory**

- Global distributed shared memory thru distributed directory table
- Dynamic page migration
- Wide registers serve as context sensitive TLB

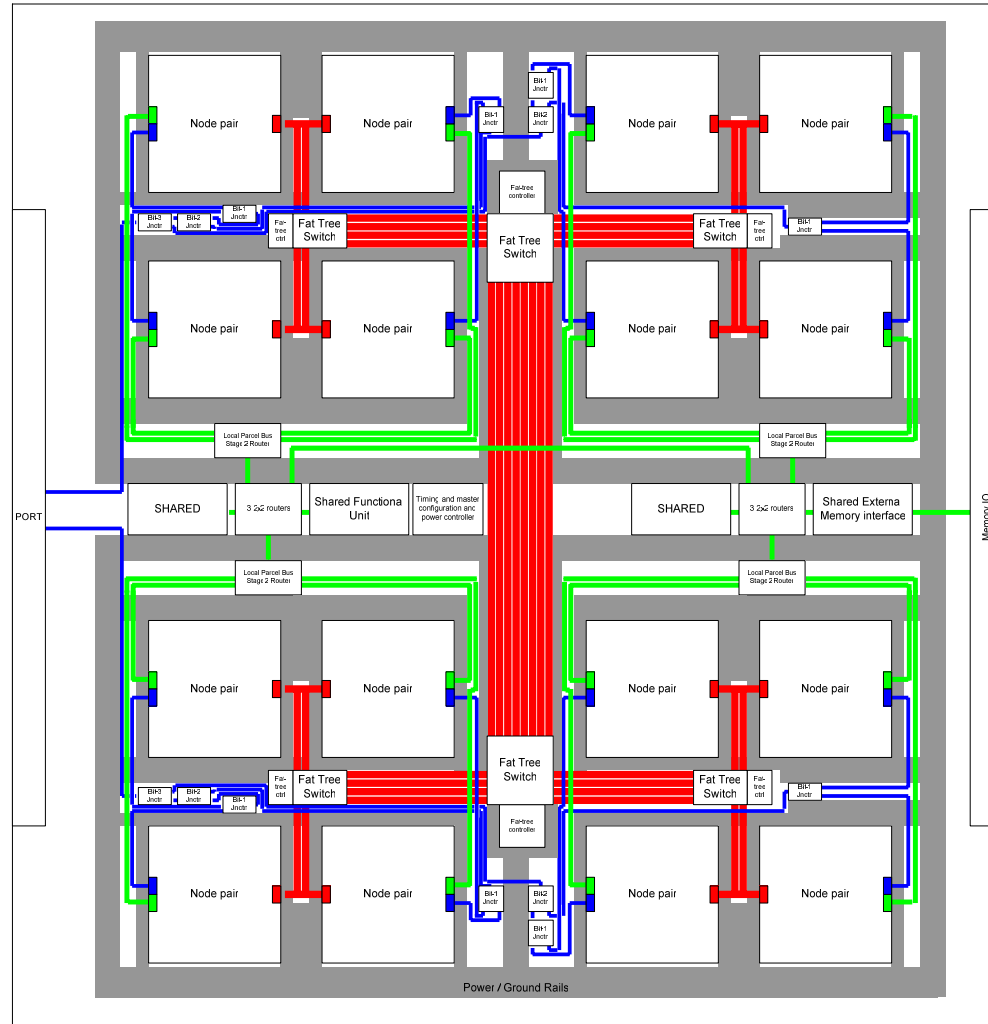
- **Graceful degradation for Fault tolerance**

- Graceful degradation through highly replicated fine-grain elements.
- Hardware architecture includes fault detection mechanisms.
- Software tags for bit-checking at hardware speeds; includes memory scrubbing.
- Virtual data and tasks permits rapid reconfiguration without software regeneration.



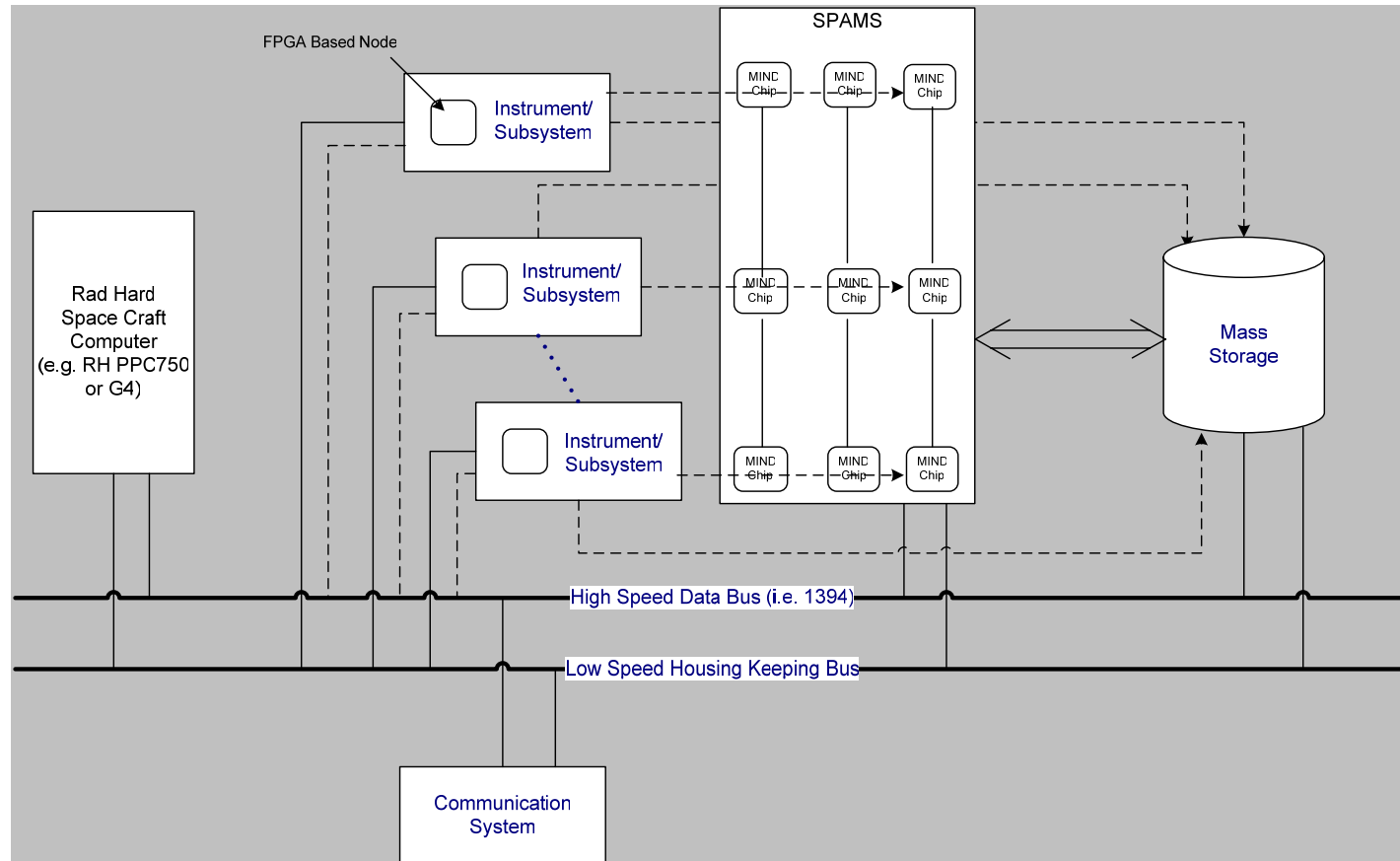


MIND Multi-Core Chip Layout





SPAMS Architecture

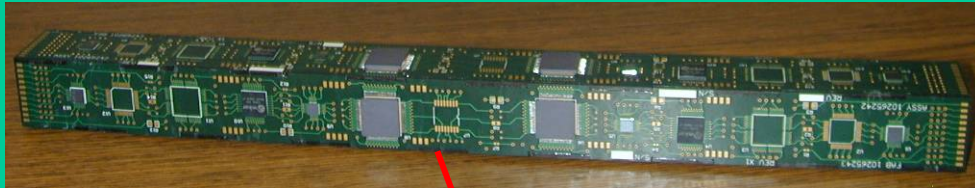
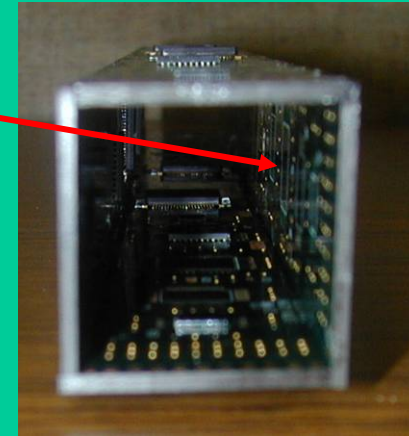




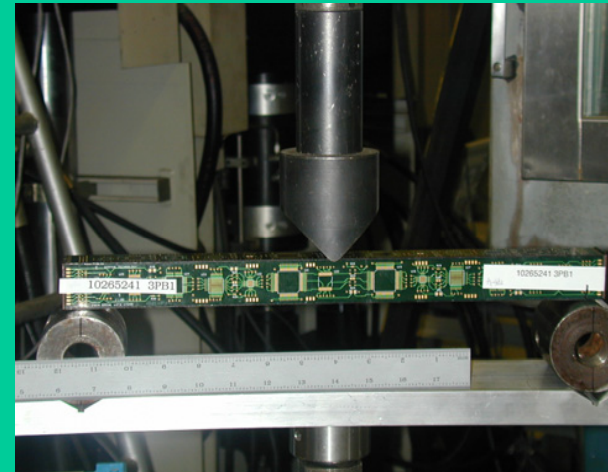
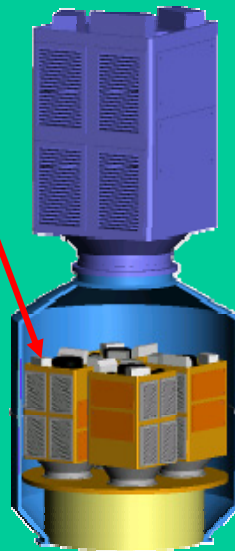
SPAMS Implementations



Wiring cables are built inside the structure elements.



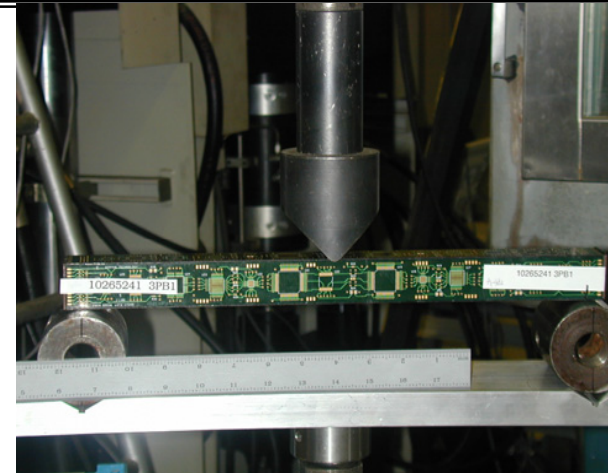
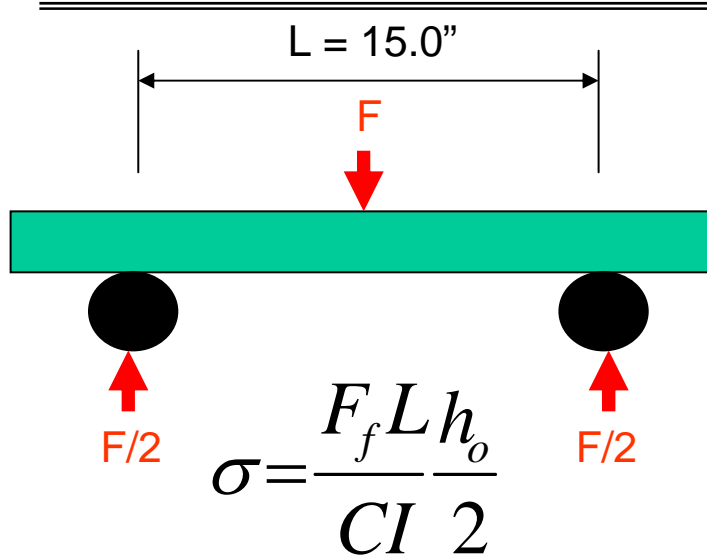
Spacecraft instrument chassis and structure members are made of fault tolerant high performance computer boards.



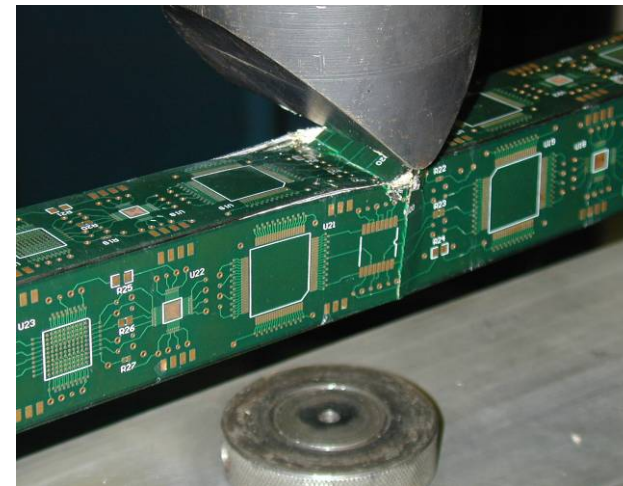
3-Point Bend Test



3-Point Bend Test: Polyimide Box Beam



Test Set-up: Start



Test Set-up: Fracture

Where:

F_f = Fracture Force

L = length

h_o = thickness of beam

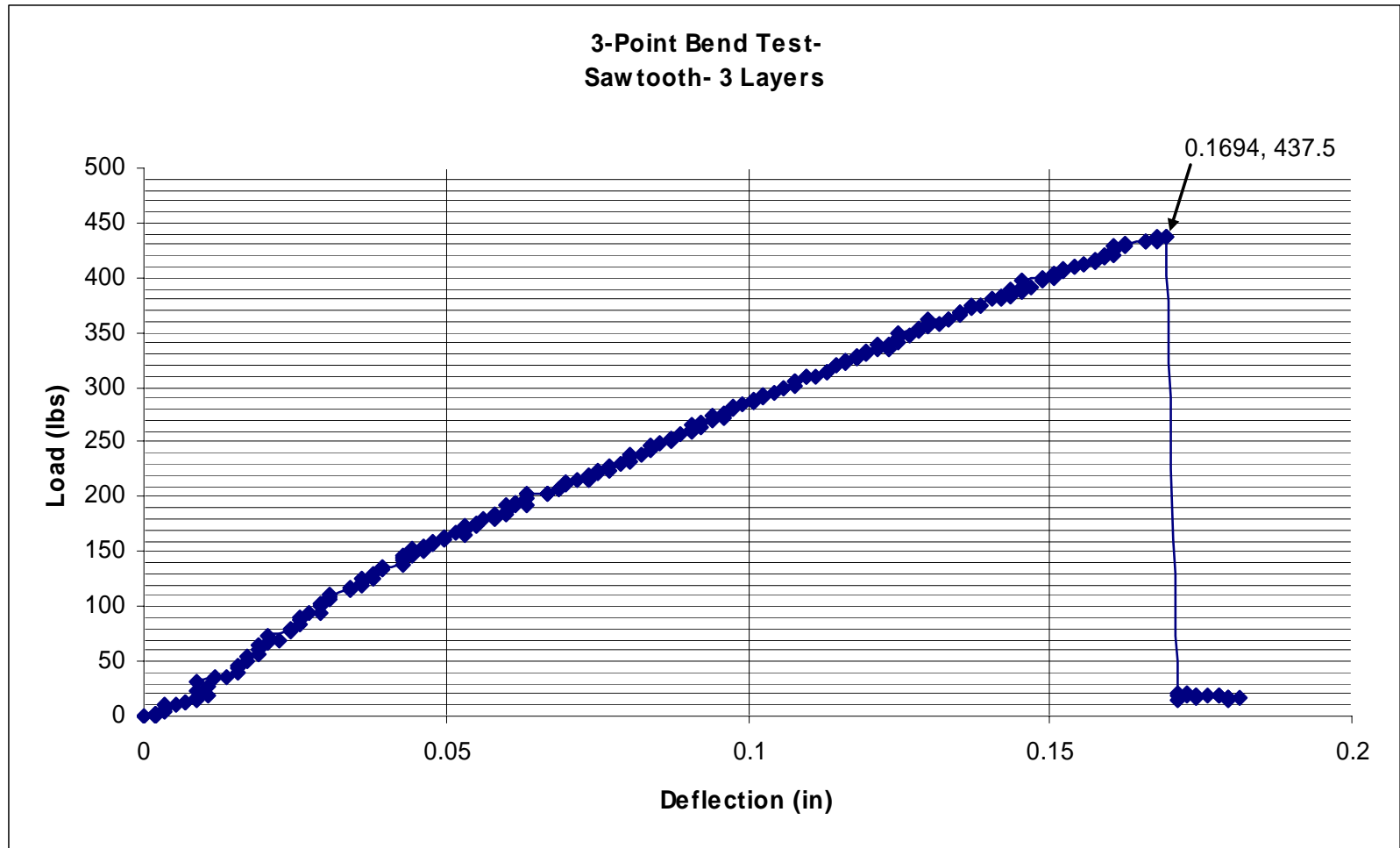
I = moment of inertia

C = constant

$C = 4$ (3-pt bend)

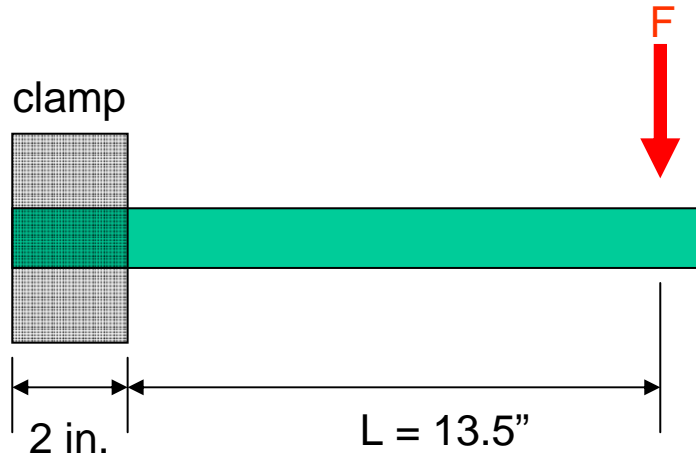


3-Point Bend Test: Polyimide Box Beam





Cantilever Test: Polyimide Box Beam



$$\sigma = \frac{F_f L h_o}{CI 2}$$

Where:

F_f = Fracture Force

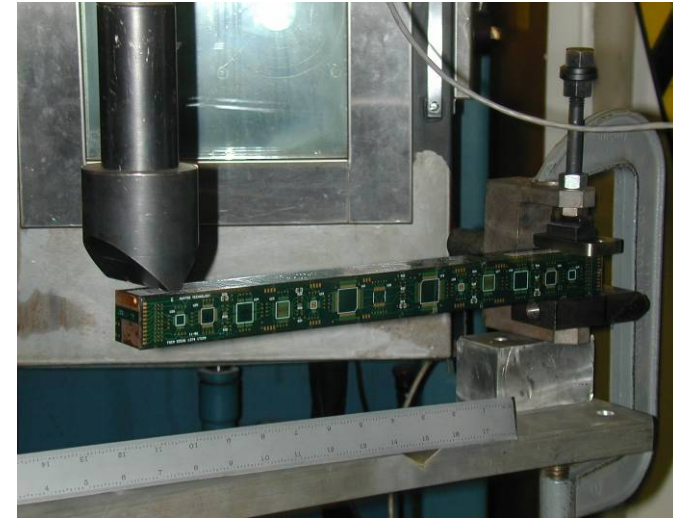
L = length

h_o = thickness of beam

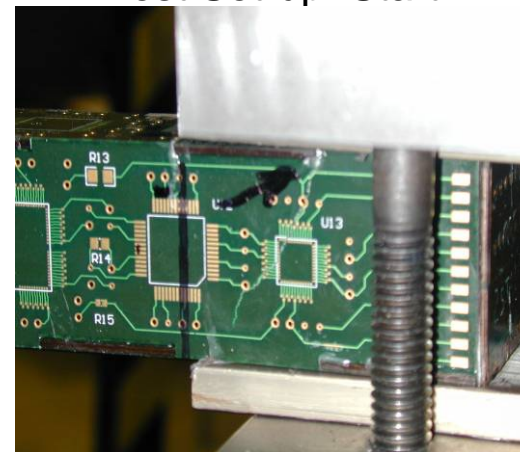
I = moment of inertia

C = constant

$C = 1$ for cantilever



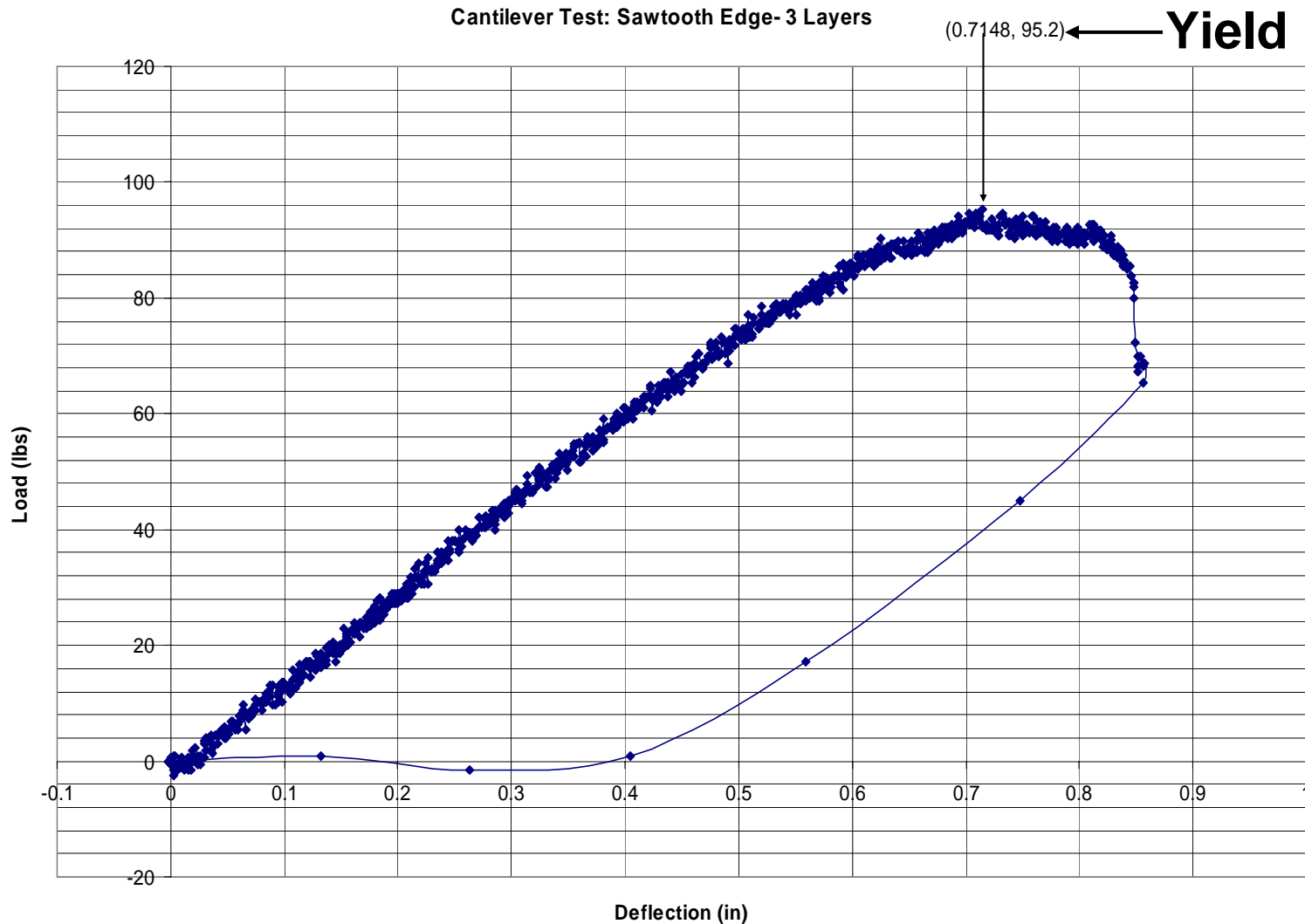
Test Set-up: Start



Test Set-up: Break



Cantilever Test: Polyimide Box Beam





Conclusion

- **SPAMS can potentially provide high performance computing to spacecraft without sacrificing additional mass.**
- **Gilgamesh architecture allows SPAMS to provide high performance, low power, and long duration fault tolerance.**
- **We are building and testing different elements of the SPAMS.**