Spaceborne Processor Array in Multifunctional Structure (SPAMS)

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1. Introduction

In the future, NASA's planetary in-situ measurement spacecrafts such as Titan or Mars Aerobots will require high performance on-board processing capability yet will be severely limited by mass. Future long duration exploration and autonomous deep-space missions will also require dramatic increases in computational performance to match the high-level goal-directed cognitive mission and contingency planning demands even as power consumption must be very low.

DoD programs such as the Space Superiority and Unmanned Aerial Vehicle require on-board processing capability. Other programs such as the Operationally Responsive Space (ORS) program requires rapidly deployable, customizable satellites with standard buses, payloads, and launchers. In order to meet the evolving threats and short deployment timeframe requirements, future DoD space and aerial vehicles will have increasing need for software reprogrammable high performance on-board processing capabilities.

Current spacecraft design typically positions electronics in a centrally located chassis that contains circuit boards interconnected to a chassis backplane. Electrical signals from the chassis are transmitted using bulky cabling configurations. In addition, structural elements are fabricated from relatively heavy metals such as aluminum and titanium. As shown in Table 1, recent developments in printed circuit board material have given printed circuit boards up to an order of magnitude increased stiffness and rigidity over currently used metallic solutions with a 30% reduction in mass.

RAW Material	Heat Thermal Conductivity	Strength Tensile Modulus	Weight Density	Thermal Expansion CTE
Carbon Graphite Composite ST325 [1]	325 (W/m*K)	114.0 (msi)	2.17 (g/cm^3)	-1.15 (ppm/C)
Polyimide [1,2]	0.3	3.0	1.70	16.50 X,Y dir
Copper [1]	385	12.0	8.92	17.00
Aluminum 100%[1]	240	10.2	2.70	24.00

Table 1: Material Property Comparison

Based on these new materials, it will be possible to construct spacecraft structural elements and electronic housing by designing electromechanical "I" beams, "Box" beams (see Figure 1) and electromechanical cardcages that will replace a conventional electronic circuit board, data / power transmission cable and an aluminum or titanium structural member. Spacecraft built with this type of Multifunctional Structure (MFS) can have significantly more computing electronics without higher mass.

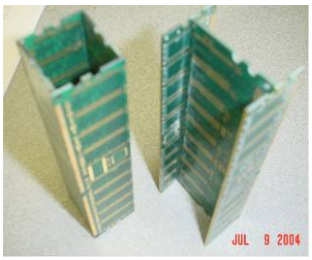

Figure 1: Models of Electromechanical "I" Beam and "Box" Beam

The goal of the SPAMS project is to enable NASA to design low mass, cost effective, fault tolerant and autonomous spaceflight hardware with supercomputing level performance for planetary in-situ measurement spacecrafts and smart sensors. Our approach is to integrate the MFS and the Gilgamesh **M***emory,* **I***ntelligence, and* **N***etwork* **D***evice* (MIND) multi-core in-memory computer architecture [3] into a single system super-architecture. The objective is to turn every inch of the spacecraft into a sharable interconnected smart computing element so that we can increase computing performance and reduce mass at the same time.

2. SPAMS System Architecture

The MIND in-memory architecture provides a foundation for high performance, low power, and fault tolerant computing [4]. The MIND chip has an internal structure that includes memory, processing, and communication functionality. The Gilgamesh is a scalable system comprising multiple MIND chips interconnected to operate as a single tightly coupled parallel computer. The array of MIND components shares a global virtual name space for program variables and tasks that are allocated at run time to the distributed physical memory and processing resources. Individual processor-memory nodes can be activated or powered-down at run time to provide active power management and to configure around faults.

The MIND chips interoperate through an active message protocol called *parcels* that supports everything from simple memory access requests to the remote invocation of entire programs with efficient light-weight transport, interpretation, and context switching mechanisms for effective handling of a range of parcel packet sizes.

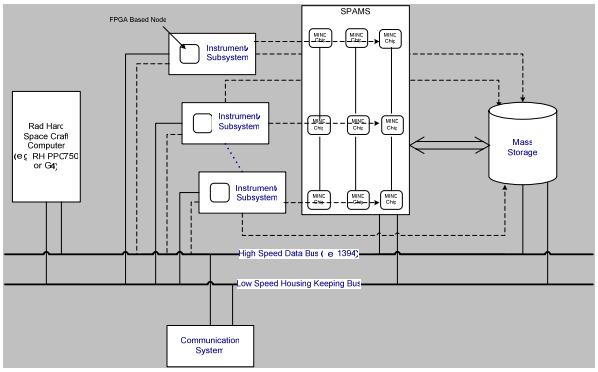

Figure 2: SPAMS System Architecture

Figure 2 depicts the high level SPAMS system architecture. A SPAMS system is comprised of distributed Gilgamesh array built into MFS, interfaces to instrument and communication subsystems, mass storage interface, and a rad hard flight computer.

Because of the low co-efficient of thermal expansion (CTE) for the new composite material, the MIND processor die can be mounted directly on the MFS printed circuit board. This enables large number of processors with minimum impact on the spacecraft mass. However, in order to efficiently utilize these processors in a SPAMS system, there are some challenging design issues; 1) Since the SPAMS processor array is distributed in the structure of the spacecraft, the size and shape of the spacecraft may impact computing performance. 2) The SPAMS processor array interconnection topology will change based on the shape of the spacecraft. 3) In order to reduce power consumption, the SPAMS processors are selectively powered on when necessary. Programming of this dynamic re-organization of ensemble of processors can be challenging. 4) Since the processors are distributed throughout the spacecraft, distributed fault tolerance capability is critical. 5) In order to reduce the system cost, the goal is to use large number of low cost, fault tolerant, non-radiation hardened processors controlled by lower performance rad hard flight computer.

Our approach to address these issues is to leverage on the architectural strength of the Gilgamesh array. The MIND parcel interconnect hardware interface supports various network structures through a programmable routing table. The MIND chips in the SPAMS system will support multiple parcel interfaces to allow maximum flexibility in interconnection topology. The Gilgamesh Macroservers and shared virtual address space allow efficient execution and simplified programming. Large number of MIND processors in the SPAMS system can enable redundancy checking to handle both transient and permanent faults.

3. Mechanical Design and Testing

A number of MFS structures have been manufactured for testing. Figure 3 shows a Polyimide box beam with 3 layers of ST-325 and sawtooth edge construction. Initial results indicate strong breaking strength. The printed circuit board also exhibits good thermal conductivity and can tolerate higher shock and vibration frequency.

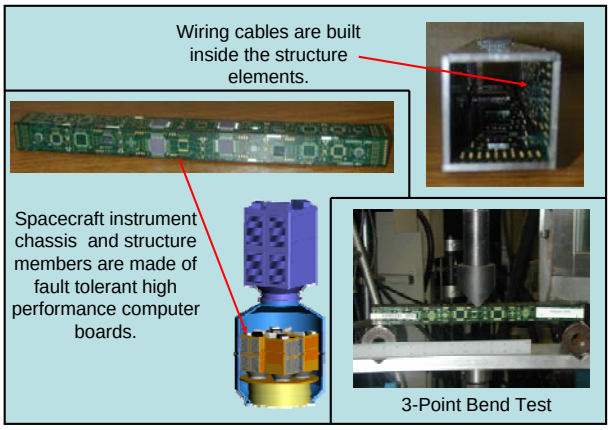

Figure 3: MFS Box Beam and Applications

4. References

[1] Thermal Works Corp., "Technology Overview", http://www.thermalworks.com

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