Algorithm Development for Future High Performance Systems using SystemCV
Jigsaw: An Early Case Study

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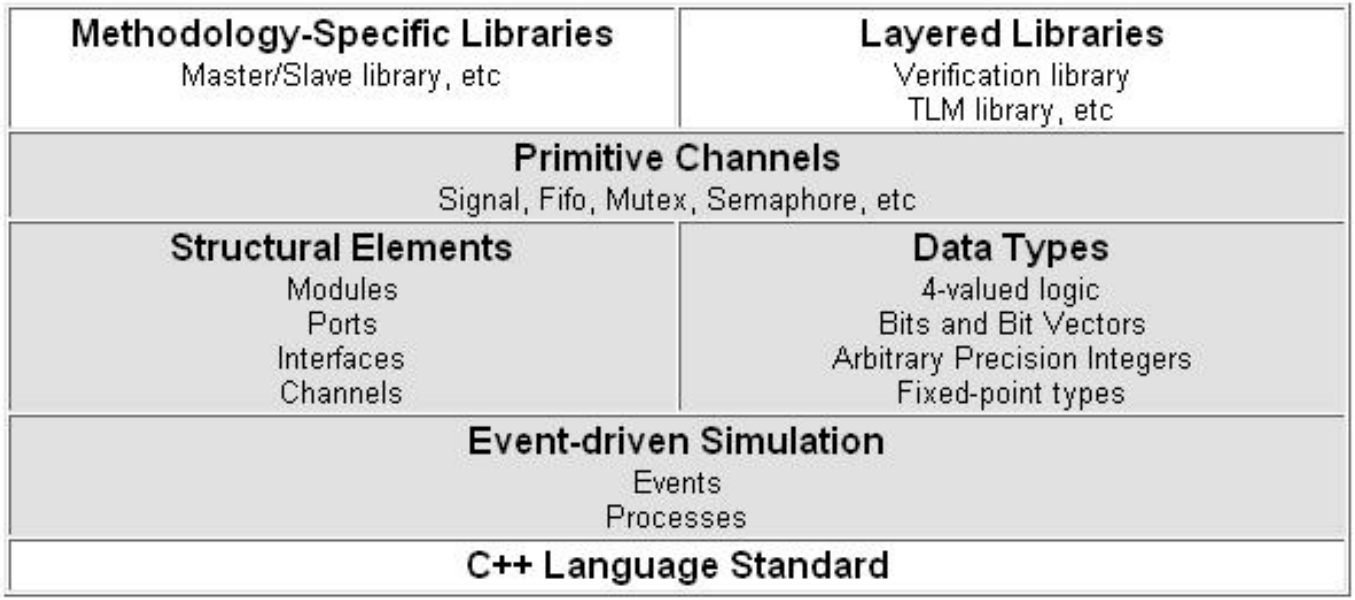
SystemC with Visualization: SystemCV

- HW/SW Simulation
- Concurrent Implementation
- Architecture exploration
- Hierarchical & modular design
- Visualization at module and system levels
- Incremental sophistication of both the communications and computational model
- IP protection

SystemCV = SystemC + Visualization Tool Kit (VTK)

SystemC Architecture

(IEEE 1666 Standard)



SystemCV Top Down Design

System Specification

Executible Spec

System Architecture

Algorithmic decomposition into modules and interfaces

Architecture Exploration

Hardware Software tradeoff
Communication model
Compute Node Type selection
External Interaction Model

Architecture Refinement

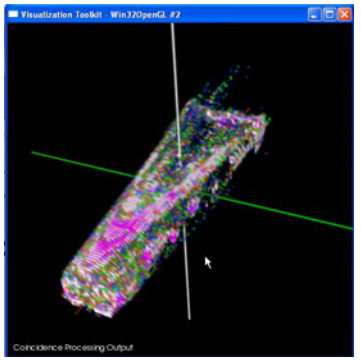
Performance Constraints
Physical Constraints
Pseudo Timing accurate model

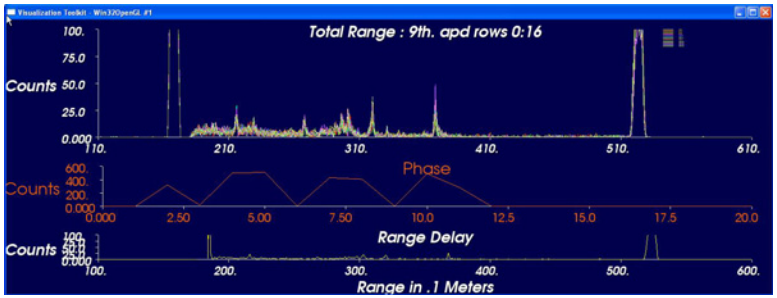
Implementation

RTL
FPGA\DSP\RISC code
Cycle accurate model

Testing & Compliance

RTL test bench





Jigsaw SystemCV