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DIFdoc: a standard format for visualizing hierarchical dataflow representations

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High Performance Embedded DSP Design

- Dataflow has been shown to be a highly intuitive and efficient conceptual and visual format
  - Formal properties (scheduling, bounded memory, etc.)
  - Hierarchical (captures complex designs)
  - Exposes parallelism
- Many commercial tools utilize dataflow for DSP system design, e.g. ...
  - Gedae
  - National Instruments LabVIEW
  - Agilent ADS

DIFdoc

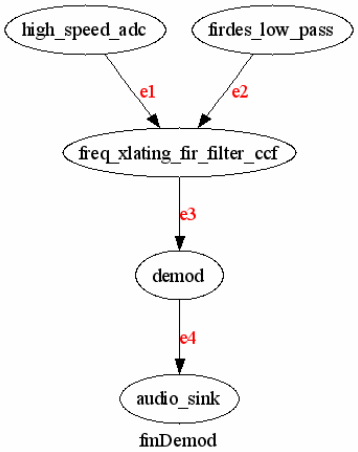
- Combined textual-pictorial representation of dataflow designs
  - Provides a unique representation of an entire dataflow hierarchy
  - Tool-independent
  - Human-readable dataflow graph documentation format
- Displays dataflow-based design hierarchies using HTML and dot
  - Indentation used to represent hierarchy
  - Pictorially represent graphs

DIFdoc Examples

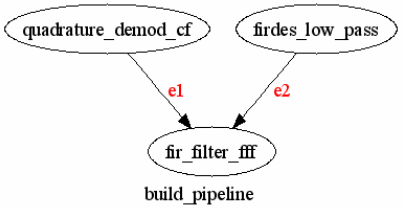
(a)

```
fmDemod
    high_speed_adc
    freq_xlating_fir_filter_ccf
    firdes_low_pass
    demod
        quadrature_demod_cf
        fir_filter_fff
        firdes_low_pass
    audio_sink
```

(b)



(c)



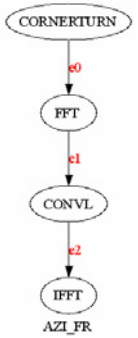
FM demodulation example from GNU radio.

(a)

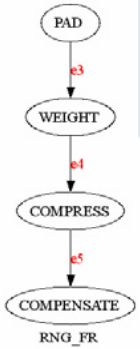
```
SAR
    SARFR
        AZI_FR
            CORNERTURN
            FFT
            CONVL
            IFFT
        RNG_FR
            PAD
            WEIGHT
            COMPRESS
            COMPENSATE
    FilterCoefReader
    SARDataReader
    FilterCoefReader2
    FilterCoefReader3
    LineWriter
```

(b)

(c)



(d)



Synthetic aperture radar example from MCCI.