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Reusing Verification Components in System-level Modeling Environments

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Verification Challenges

- Verification extremely complex
  - Complex distributed software architecture
  - Multiple domains
- State of the art
  - System-level modeling
    - Simulink®
  - Verification
    - Hardware Verification Languages
      - SystemVerilog, SystemC, e, Vera
    - Reuse-based methodologies
      - AVM, VMM, URM

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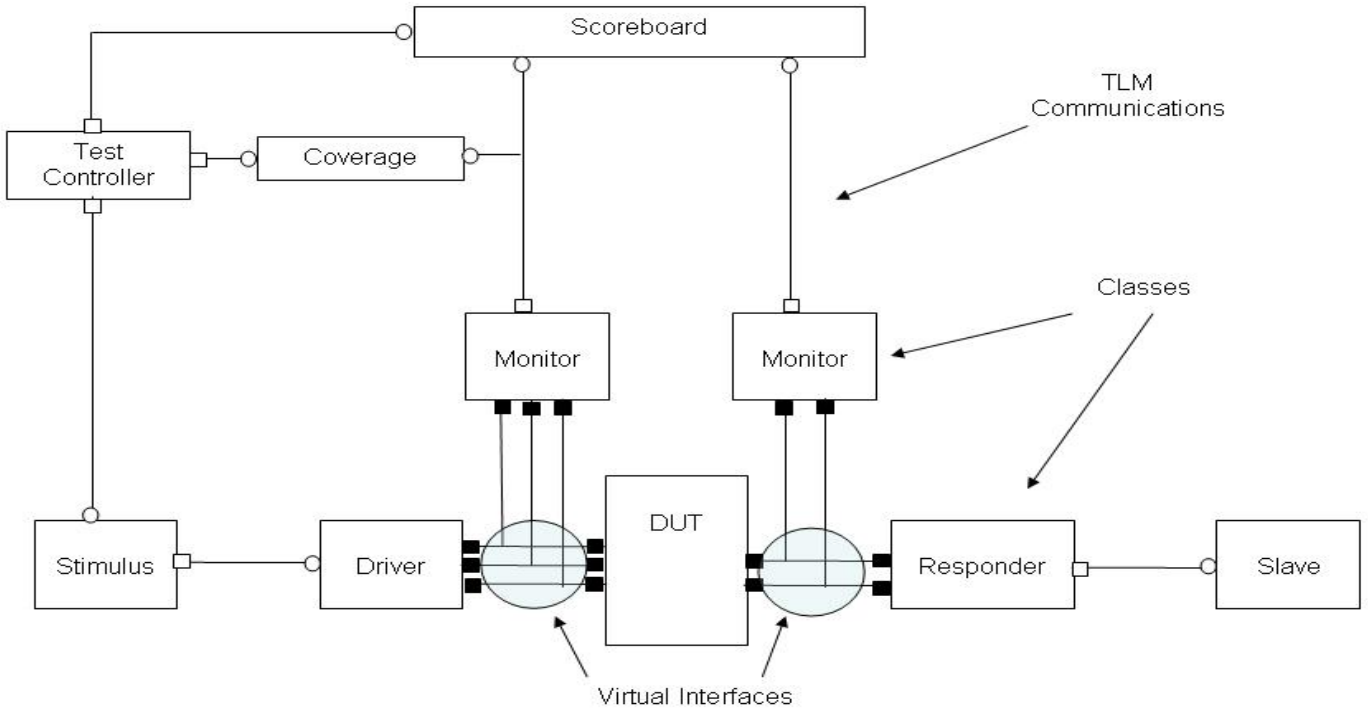
AVM- A Reuse Based Verification Environment



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Integrating AVM and Simulink®