



The HPEC Challenge Benchmark Suite

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Motivation

Advanced Sensor Platforms



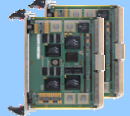
Processor and System Architectures



Single Processor
Element



Tiled
Processors



Multi-
computers

System Analysis and Design

Implement Benchmarks

- Design
- Code
- Tune

Measure Performance

- Throughput
- Power
- Stability

Design System

- Choose components
- Hardware size
- Required software performance

HPEC Challenge Benchmark Suite

- **Kernel Benchmarks**
 - Single-processor operations
 - Taken from PCA program
- **SAR Application Benchmark**
 - Multi-processor compact application
 - Taken from HPCS program



Outline



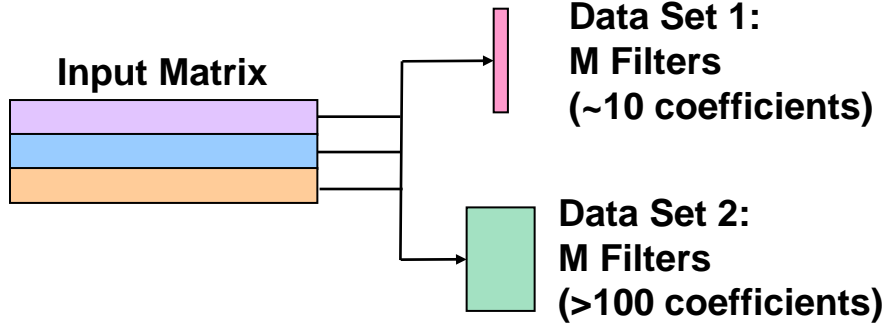
- Motivation
- • **Benchmark Suite**
 - Kernel Benchmarks
 - SAR Application Benchmark
- Web Site



Signal and Image Processing Kernels

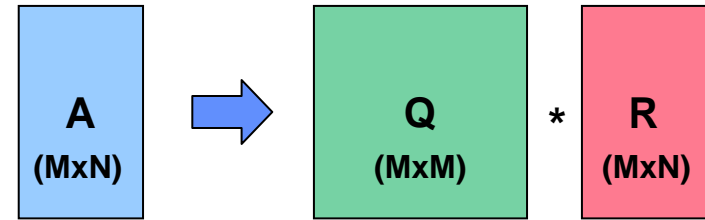
FIR

M Channels



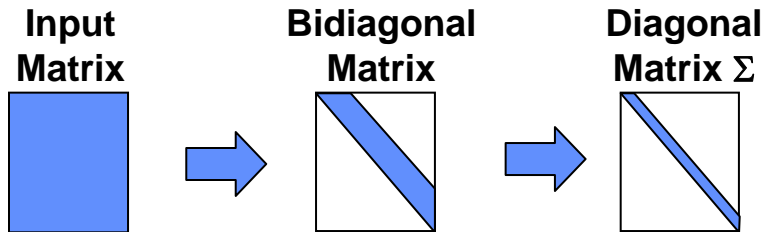
- Bank of filters applied to input data
- FIR filters implemented in time and frequency domain

QR



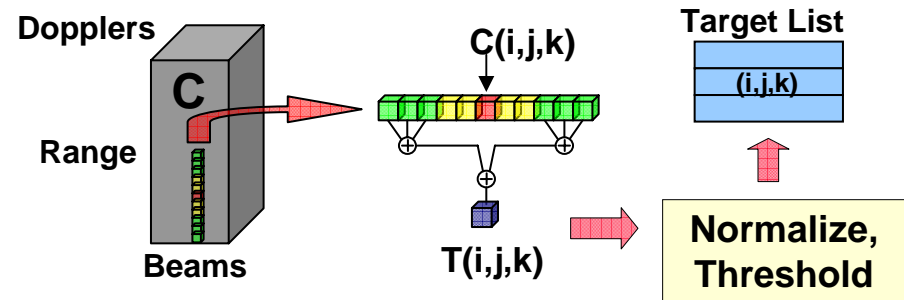
- Computes the factorization of an input matrix, $A=QR$
- Implementation uses Fast Givens algorithm

SVD

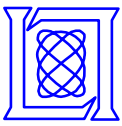


- Produces decomposition of an input matrix, $X=U\Sigma V^H$
- Classic Golub-Kahan SVD implementation

CFAR

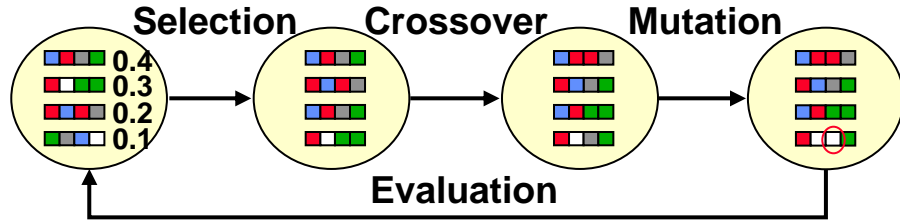


- Creates a target list given a data cube
- Calculates normalized power for each cell, thresholds for target detection



Information and Knowledge Processing Kernels

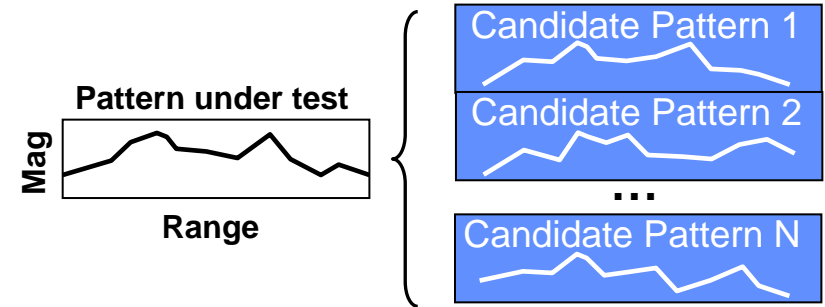
Genetic Algorithm



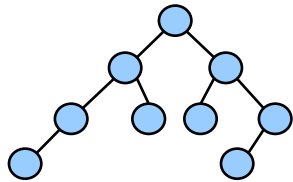
- Evaluate each chromosome
- Select chromosomes for next generation
- Crossover: randomly pair up chromosomes and exchange portions
- Mutation: randomly change each chromosome

Pattern Match

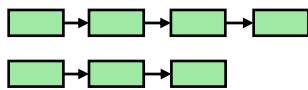
- Compute best match for a pattern out of set of candidate patterns
 - Uses weighted mean-square error



Database Operations



Red-Black Tree Data Structure



Linked List Data Structures

- Three generic database operations:
 - search: find all items in a given range
 - insert: add items to the database
 - delete: remove item from the database

Corner Turn

0	1	2	3
4	5	6	7
8	9	10	11

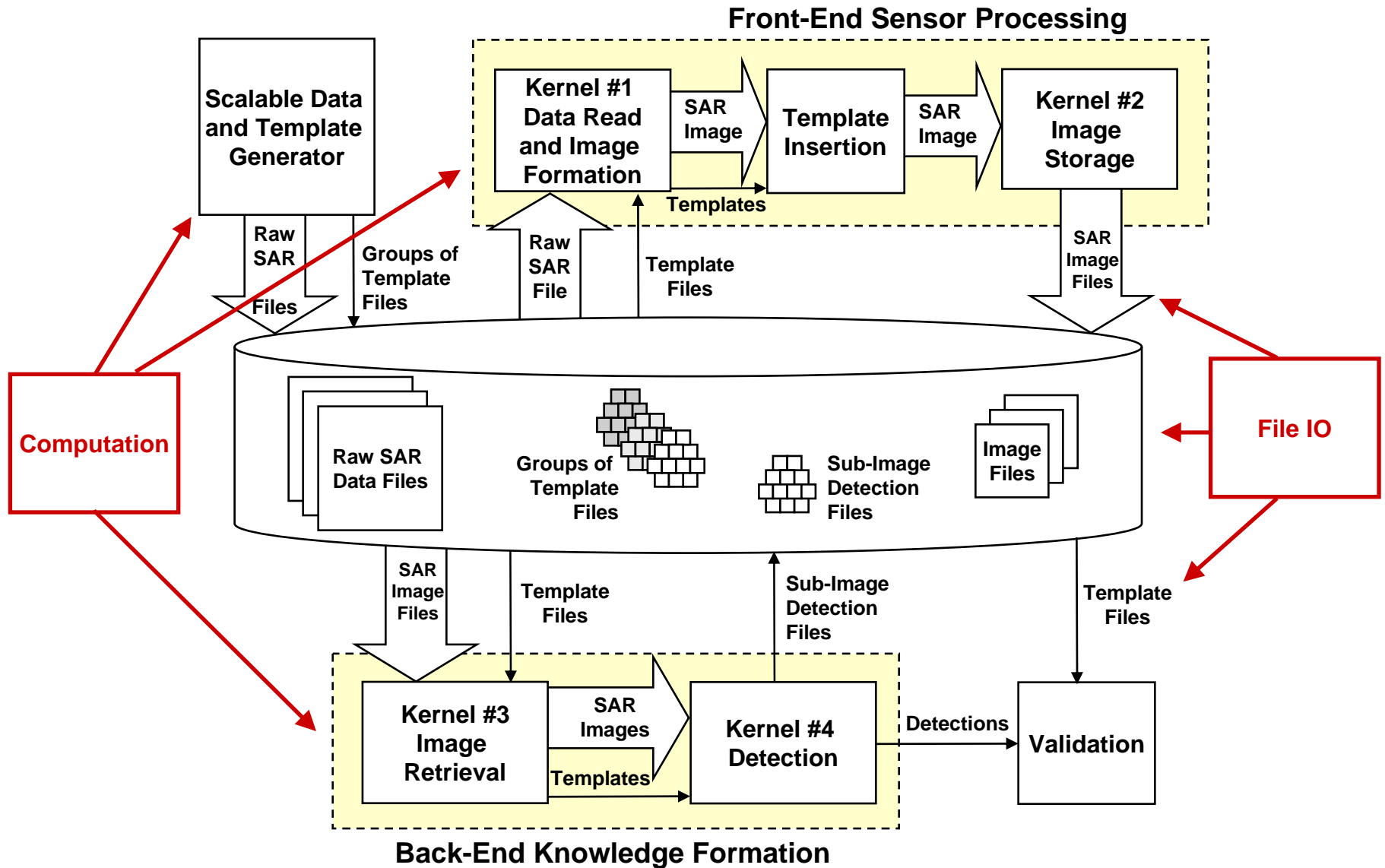


0	4	8
1	5	9
2	6	10
3	7	11

- Memory rearrangement of matrix contents
 - Switch from row to column major layout

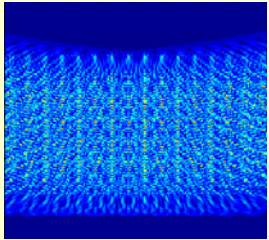
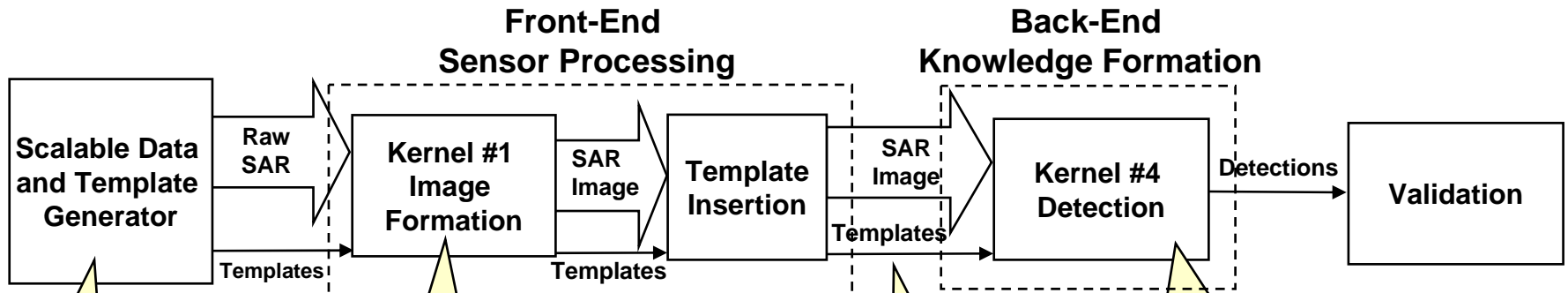


SAR System Architecture

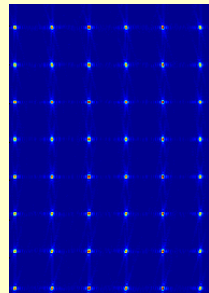




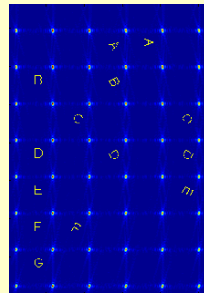
SAR Benchmark Computational Challenges and Data Products



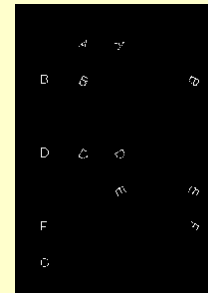
- Scalable synthetic data generation



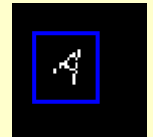
- Pulse compression
- Polar Interpolation
- FFT, IFFT (corner turn)



- Sequential store
- Non-sequential retrieve
- Large & small IO



- Large Images difference & Threshold

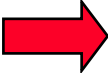


- Many small correlations on random pieces of large image



Outline



- **Motivation**
- **Benchmark Suite**
 - Kernel Benchmarks
 - SAR Application Benchmark
-  • **Web Site**



- **Purpose:**
 - Allow exploration of performance results for a wide range of architectures
- **Provide public and password protected pages**
 - Secure potentially sensitive architecture results
- **Public pages:**
 - Benchmark information
 - Benchmark software
 - Periodic releases of benchmark results

The screenshot shows the HPEC Challenge website. The header features the text "hpecchallenge" in a large, stylized font. Below the header is a navigation menu with links for Home, Benchmarks, Software, Publications, Acknowledgments, Site Map, and Login/Register. The main content area is titled "Introducing the HPEC Challenge Benchmark Suite" and contains several paragraphs of text. The text discusses the challenges of producing software, firmware, and hardware for high performance commercial and DoD applications, and introduces a suite of benchmarks for evaluation. It also provides information on how to access the benchmarks and software, and how to contact the project.

Introducing the HPEC Challenge Benchmark Suite

The embedded computing community is faced with an ever increasing challenge of producing software, firmware, and hardware to meet the demands of high performance commercial and DoD applications. These application requirements are driving the use of new computer processing elements with new processor architectures and increasing the complexity of application software.

To provide a means to quantitatively evaluate such high performance embedded computing (HPEC) systems, we propose a challenge to the community in the form of a suite of benchmarks. The HPEC Challenge benchmark suite consists of a set of single-processor kernel benchmarks and a multi-processor application benchmark. The kernel benchmarks address important operations across a broad range of DoD signal and image processing applications. The application benchmark implements a scalable Synthetic Aperture Radar (SAR) application that is representative of one of the most common functions in DoD surveillance systems.

More information on the benchmarks is provided on the [Benchmark](#) page. Links to benchmark description pages can also be found below. The HPEC Challenge software distribution can be found on the [Software](#) page. Viewing or posting benchmark results to this web site requires registration to the site. Go to the [Registration](#) page to obtain a username and password.

The HPEC Challenge benchmarks and web site are works in progress. Please contact hpecChallenge@ll.mit.edu with any comments, questions, or suggestions for improvement.

Kernel Benchmarks

1. Time-Domain Finite Impulse Response Filter Bank - TDFIR
2. Frequency-Domain Finite Impulse Response Filter Bank - FDFIR
3. QR Factorization - QR
4. Singular Value Decomposition - SVD
5. Constant False-Alarm Rate Detection - CFAR
6. Pattern Matching - PM
7. Genetic Algorithm - GA
8. Database Operations - DB
9. Corner Turn - CT

Multi-Processor Application Benchmark

1. Synthetic Aperture Radar - SAR

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Benchmark Information



Home | Benchmarks | Software | Publications | Acknowledgments

Benchmarks

The HPEC Challenge benchmark suite consists of a set of eight kernel benchmarks and a system benchmark for quantitatively comparing HPEC systems. The kernel benchmarks cover a broad range of DoD signal and image processing applications. The scalable SAR is one of the most common functions in DoD surveillance systems. In addition, it includes several other classes of applications.

Metrics of interest for the benchmarks are defined on the metrics page.

Kernel Benchmarks

1. Time-Domain Finite Impulse Response Filter Bank - TDFIR
2. Frequency-Domain Finite Impulse Response Filter Bank - FDFIR
3. QR factorization - QR
4. Singular Value Decomposition - SVD
5. Constant False-Alarm Rate Detection - CFAR
6. Pattern Matching - PM
7. Genetic Algorithm - GA
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9. Corner Turn - CT

Multi-Processor Application Benchmark

1. Synthetic Aperture Radar - SAR

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Time-Domain Finite Impulse Response Filter Bank

The finite impulse response (FIR) filter is one of the basic operations in signal processing. This kernel implements a set of M FIR filters. Each FIR filter m, m ∈ {0, 1, ..., M-1}, has a set of impulse response coefficients w_m[k], k ∈ {0 ... K-1}. If the length of the input vector is N, the output of filter m, y_m, is the convolution of w_m with the input x_m:

$$y_m[i] = \sum_{k=0}^{K-1} x_m[i-k]w_m[k], \text{ for } i = 0, 1, \dots, N-1.$$

We define two datasets in Table 1, one for a short filter and one for a long filter.

Table 1: FIR filter bank input parameters.

Parameter Name	Description	Values	
		Set 1	Set 2

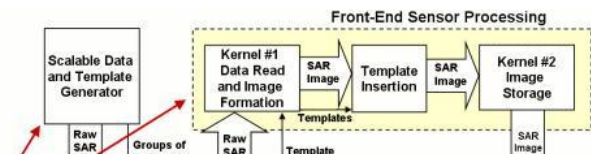
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SAR Benchmark

The HPCS Scalable Synthetic Compact Application #3 (SSCA #3) simulates a sensor processing chain (Figure 1). It consists of a front-end sensor processing stage, where Synthetic Aperture Radar (SAR) images are formed, and a back-end knowledge formation stage, where detection is performed on the difference of the SAR images. It generates its own synthetic 'raw' data, which is scalable. The goal is to mimic the most taxing computation and I/O requirements found in many embedded systems, such as medical/space imaging, or reconnaissance monitoring. Its principal performance goal is throughput, in other words, to maximize the rate at which answers are generated. The computational kernels must keep up with copious quantities of sensor data. Its I/O kernels must manage both streaming data storage, as well as sequential file retrieval.





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Software

- Download: [HPEC Challenge Benchmark Suite v1.0 \(Kernel Benchmarks only\)](#)
- Download: [HPEC Challenge SAR Benchmark v1.0 \(Found under SSCA #3 v1.0\)](#)

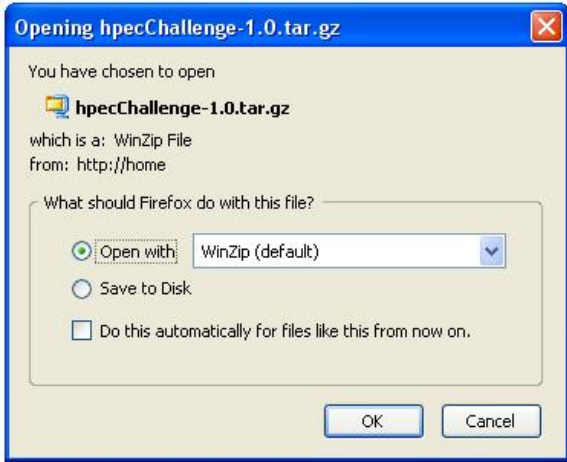
Contents:

Version 1.0 of the benchmark suite download contains the kernel-level benchmarks only. A future release will SAR multi-processor application benchmark. Information on the Kernel-level benchmarks may be found on the page. For now, the SAR benchmark must be downloaded from the HPCS program web page. This will require the HPCS program.

Software Instructions

Kernel Benchmarks

The following descriptions and instructions can be found in the README.txt file found in the hpecChallenge/kernelBenchmark directory after unzipping the software distribution file. To unzip the distribution file, use winzip in Windows, or "gunzip file.tar.gz; tar xvf file.tar" in Unix.





- Registration
 - Obtain username, access to password protected pages
- Password protected pages:
 - Upload results to site
 - Architecture results, reports

First Name	Ryan
Last Name	Haney
User Name	haney
Password	*****
Organization	MIT Lincoln Laboratory
Email	haney@ll.mit.edu
Phone	781-981-5500
Country of citizenship	U.S.A.
Area of Work	Government
Reason for use	High performance embedded computing research for the MIT Lincoln Laboratory Embedded Digital Systems Group.]

Submit

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Uploading Results

hpecchallenge

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Welcome Ryan Haney

This page allows a user to upload benchmark results to the HPEC Challenge website to be shared with other users. To upload results to the website, you must first enter information on the system that was benchmarked. The following sections allow you to add a new system along with relevant benchmark results to the site, or edit an existing system that you have added in the past.

Create a New System

The following link will prompt you for general information concerning the benchmarked system. A subsequent page will allow you to add more specific configuration details, and the actual benchmark results. No information will be viewable by other users until submitted to the site. This option will be provided on a subsequent page. System and result information may be deleted and removed from the site at any time.

- Create New System

Edit an Existing System

The following links allow you to add or edit system configurations already added to the site.

- Mercury PowerPC G4 System - 500 MHz G4 processor. Future documentat...
- Intel Xeon System - 2.8GHz Xeon processor....

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- Step 1
 - Create a new system
 - i.e. Describe the system you benchmarked

hpecchallenge

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Step 1: General System Info

Name:	testSystem
Interconnect:	Gigabit Ethernet
Total Power (W):	50
Description:	This is my description.
System Diagram/Picture:	<input type="button" value="Browse..."/>
Associated Publication/Document:	<input type="button" value="Browse..."/>

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Uploading Results

- Step 2
 - Fill in more detailed system specifications

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testSystem

System Overview

submit edit delete

User	Ryan Haney
Organization	MIT Lincoln Laboratory
Interconnect	Ethernet :
Total Power (W)	50
Description	This is a test.
System Diagram/Picture	
Associated Publication/Document	
Date Created	2006-08-04 19:19:24
Date Modified	2006-08-04 19:19:24

What Now?

1. Enter in the information about the system's configuration.
2. Upload or manually enter the results the system achieved on the HPEC Challenge benchmark suite.
3. Submit for review. The system information and results will not be publicly viewable until it has been submitted.

Board/Node 1

edit delete

Processors

+ Add Processor

Off-Chip Memory

+ Add Memory

+ Add Board

Optimized Code Results

Reference Code Results

Upload Results

Add/Edit Results

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Step 2: testSystem Processor Info

Quantity:	1
Name:	PowerPCG4
Vendor:	Motorola
Class:	General purpose
Model/Family:	7410
Year Introduced:	2002
Clock Speed (MHz):	500
Peak Throughput (Mflop/s):	4000
Typical Power Usage (W):	5
Data bit width:	32
Available Arithmetic:	Floating point
CMOS Process Technology (micron):	0.18
Die size (mm ²):	52
Transistors (x 10 ⁶):	10
On-Chip L1 Cache (KByte):	32
On-Chip L2 Cache (KByte):	2000
On-Chip L3 Cache (KByte):	
Off-chip Cache (KByte):	
Off-chip Bandwidth (MByte/s):	1000
Description:	

save cancel

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Uploading Results

- Step 3
 - Upload results from benchmark results file, or manually fill in

hpecchallenge

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testSystem

System Overview

submit edit delete

User	Ryan Haney
Organization	MIT Lincoln Laboratory
Interconnect	Ethernet :
Total Power (W)	50
Description	This is a test.
System Diagram/Picture	
Associated Publication/Document	
Date Created	2006-08-04 19:19:24
Date Modified	2006-08-04 19:19:24

What Now?

1. Enter in the information about the system's configuration.
2. Upload or manually enter the results the system achieved on the HPEC Challenge benchmark suite.
3. Submit for review. The system information and results will not be publicly viewable until it has been submitted.

Board/Node 1

edit delete

Processors

+ Add Processor

Off-Chip Memory

+ Add Memory
+ Add Board

Optimized Code Results

Reference Code Results

Upload Results
Add/Edit Results

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Upload results for: testSystem

Use the following to upload a results file (in the form of hpecKernelResults-<date>.txt), or manually enter results. See the [Software](#) page for instructions on running the benchmarks.

Optimized Code vs Reference Code: Optimized

File:

Contact hpecChallenge@ll.mit.edu
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Benchmark Results: Manual Entry

Benchmark	Dataset	Reference Code Latency (s)	Optimized Code Latency (s)
TDFIR	1		
	2		
FDFIR	1		
	2		
QR	1		
	2		
	3		
CFAR	1		
	2		
	3		
	4		
PM	1		
	2		
GA	1		
	2		
	3		
	4		
CT	1		
	2		
DB	1		
	2		



Viewing Results



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Results

For more information on the metrics used on the Results pages, see the metrics document.

System	TDFIR (Mflop/s)	FD FIR (Mflop/s)	QR (Mflop/s)	SVD (Mflop/s)	CFAR (Mflop/s)	PM (Mflop/s)	GA (Mflop/s)
Mercury PowerPC G4 System	1027.000	779.000	603.667	360.000	141.947	115.500	1.000
Intel Xeon System	232.20					45.6	

User: Ryan Haney
 Organization: MIT Lincoln Laboratory
 Interconnect: Other
 Description: See attached documentation for system specifications and benchmark implementation and results details.
 Date Created: 2006-06-26 11:37:54
 Date Updated: 2006-06-26 17:59:19

* System and results have not been verified.

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Mercury PowerPC G4 System

Optimized Code Results

Benchmark	Dataset	Workload (Mflop)	Latency (s)	Throughput (Mflop/s)	Throughput/Watt (Mflop/s/W)	Stability
Time Domain FIR Filter Bank (TDFIR)	1	1.97	0.0019	1027.0	205.4	1.000
	2	30.53	0.0505	604.0	120.8	
Frequency Domain FIR Filter Bank (FD FIR)	1	33.55	0.0431	779.0	155.8	1.000
	2	397.33	0.6440	617.0	123.4	0.956
	3	45.00	0.0763	590.0	118.0	
Singular Value Decomposition (SVD)	1	125.63	0.2725	461.0	92.2	0.464
	2	20.27	0.0500	405.0	81.0	
	3	153.67	0.7181	214.0	42.8	
Constant False-Alarm Rate Detection (CFAR)	1	0.17	0.0011	156.0	31.2	0.864
	3	41.05	0.3044	134.8	27.0	
	4	17.74	0.1314	135.0	27.0	
Pattern Matching (PM)	1	1.20	0.0105	115.0	23.0	0.991
	2	13.59	0.1172	116.0	23.2	
Genetic Algorithm (GA)	1	0.01	0.0001	149.9	30.0	0.311
	2	0.50	0.0025	203.5	40.7	
	3	0.02	0.0002	96.5	19.3	
	4	0.11	0.0018	63.3	12.7	

- General comparisons between architectures
- Detailed results and specifications for architectures



Summary



- **The HPEC Challenge is a publicly available suite of benchmarks for the embedded space**
 - Representative of a wide variety of DoD applications
- **Benchmarks stress computation, communication and I/O**
- **Benchmarks are provided at multiple levels**
 - Kernel: small enough to easily understand and optimize
 - Compact application: representative of real workloads
 - Single-processor and multi-processor
- **See <http://www.ll.mit.edu/HPECchallenge/> for benchmark documentation and software**
- **[Please send feedback to hpecChallenge@ll.mit.edu](mailto:hpecChallenge@ll.mit.edu)**