# The HPEC Challenge Benchmark Suite

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## Abstract

Quantitative evaluation of different multi-processor high performance embedded computing (HPEC) systems is an ongoing challenge for the HPEC community. The DARPA Polymorphous Computer Architecture (PCA) and High-Productivity Computing Systems (HPCS) programs have created kernel and system level benchmarks and metrics for comparing the different architectures being developed under these programs. This set of benchmarks, the HPEC Challenge Benchmarks, was introduced to the community in September, 2005 [1]. In this talk, we will give an overview of the benchmarks and introduce a web page that has been developed for the benchmark suite. The HPEC Challenge will enable the objective comparison of HPEC systems on a rigorous set of benchmarks.

## Kernel Benchmarks

The single-processor kernel benchmarks are drawn from a survey of several broad DoD signal processing application areas, including radar and sonar processing, infrared sensing, hyper-spectral imaging, signal intelligence, communication, and data fusion. From these applications we distilled a set of nine kernel benchmarks and data sets that are representative of the computing needs of these applications. These kernels are drawn both from "front-end" signal processing systems that operate in a data-independent fashion, as well as "back-end" information and knowledge processing systems that operate in a data-dependent fashion. The signal processing kernels are a time-domain and frequency-domain implementation of finite impulse response filtering (TDFIR and FDFIR), QR factorization (QR), singular value decomposition (SVD), and constant false-alarm rate detection (CFAR). The information and knowledge processing kernels are pattern matching (PM), graph optimization via genetic algorithm (GA), and real-time database operation (DB). The final kernel is a communication benchmark consisting of a memory re-arrangement or corner turn (CT) of a data matrix. We describe the kernels and their associated data sets in an MIT/LL project report [2].

## SAR System Benchmark

The HPCS Scalable Synthetic Compact Application #3 (SSCA #3) simulates a sensor processing chain (Figure 1). It consists of a front-end sensor processing stage, where Synthetic Aperture Radar (SAR) images are formed, and a back-end knowledge formation stage, where detection is performed on the difference of the SAR images. It generates its own synthetic 'raw' data, which is scalable. The goal is to mimic the most taxing computation and I/O requirements found in many embedded systems, such as medical/space imaging, or reconnaissance monitoring. Its principal performance goal is throughput, in other words, to maximize the rate at which answers are generated. The computational kernels must keep up with copious quantities of sensor data. Its I/O kernels must manage both streaming data storage, as well as file sequences retrieval.

The SAR system benchmark can be operated in one of three modes: System Mode (which includes both its computational kernels and I/O kernels), Compute Mode (which includes its computational kernels while bypassing its I/O kernels), and Data I/O Mode (which includes its I/O kernels while bypassing its computational kernels). Each kernel's operation is timed.

The performance of Compute Mode corresponds to the traditional focus of the HPEC community. The System Mode can be used to measure both compute and storage I/O throughput, which is becoming increasingly important in HPEC systems.

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The benchmark has been implemented both serially and in parallel. All of its computation and I/O kernels are designed to be run on parallel computing and parallel storage systems.

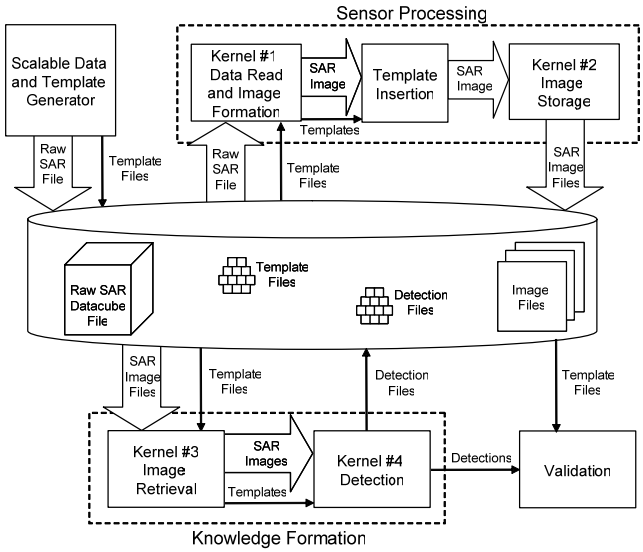


**Figure 1. Block diagram of SAR system benchmark.**

## HPEC Challenge Web Site

Benchmark software and documentation is available to the public through the HPEC Challenge web site, http://www.ll.mit.edu/hpecChallenge. The web site also provides a means for collaboration between HPEC researchers, contractors and vendors, by allowing users to post benchmark results to the site. Users can post system specifications, results obtained from running the HPEC Challenge benchmarks, and any related publications.

## Summary

We have developed a set of nine kernel benchmarks and a scalable SAR system benchmark for quantitatively comparing HPEC systems. The kernels address important operations across a broad range of DoD signal and image processing applications. The scalable SAR system benchmark is representative of one of the most common functions in DoD surveillance systems. In addition, it includes storage I/O components found in a broad class of applications. The HPEC Challenge provides the community with a valuable tool for objectively evaluating systems and the potential impact of new technologies.

## References


[1] Ryan Haney, Theresa Meuse, Jeremy Kepner and James Lebak. The HPEC Challenge Benchmark Suite. In *Proceedings of the Ninth Annual High-Performance Embedded Computing Workshop (HPEC 2005)*, Lexington, MA, September 2005.

[2] James Lebak, Albert Reuther, and Edmund Wong. Polymorphous Computing Architecture (PCA) Kernel-level Benchmarks. Project Report PCA-KERNEL-1, MIT Lincoln Laboratory, Lexington, MA, January 2004.