High Performance Low Density Parity Check and Turbo Decoding FPGA Implementation

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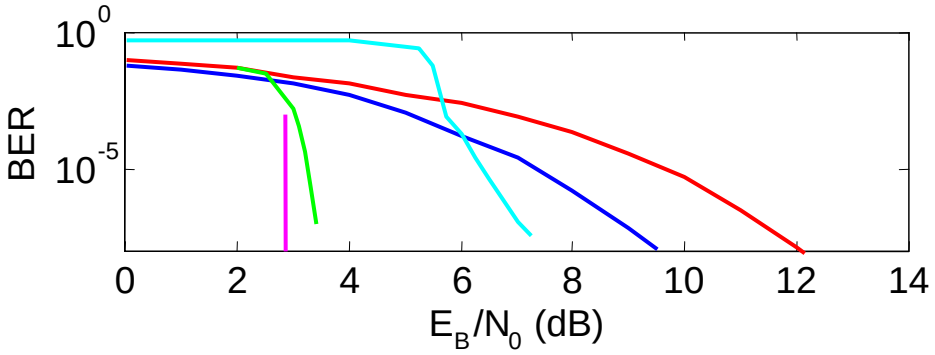
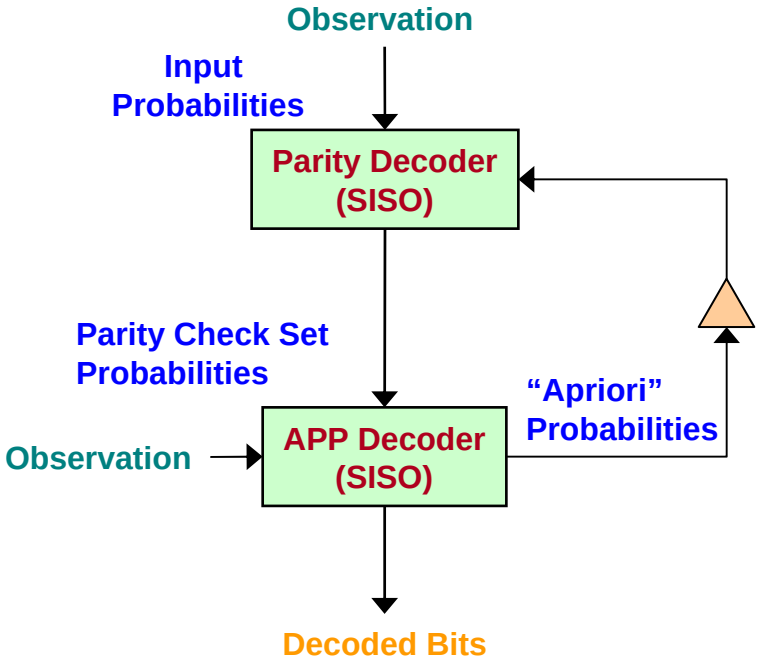
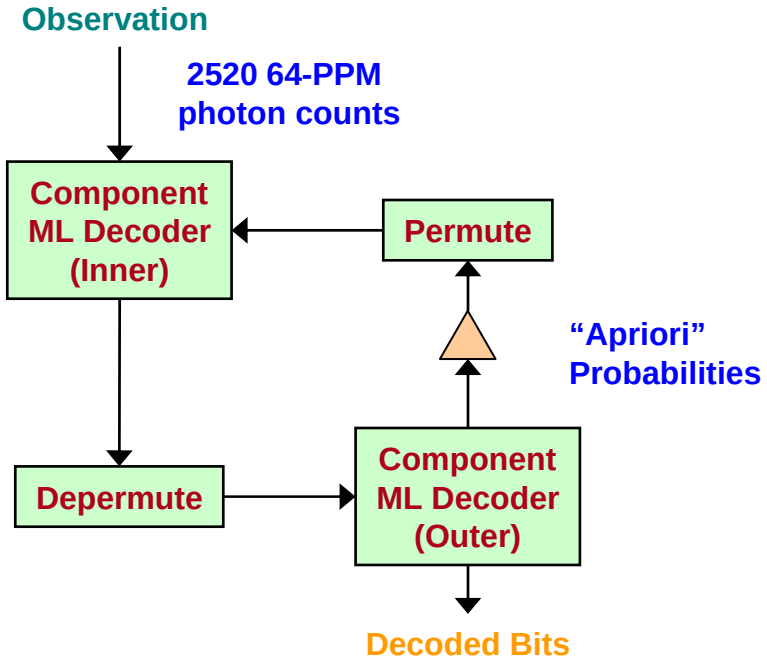
Maximizing Throughput

- Balance of component decoders
- Pooling
- Max log MAP algorithm
- Scaling of APPs
- Simultaneous decoding of codewords
- Use of LLRs

Maximize Throughput







LDPC

- **Balance of component decoders**
- **Pooling**
- Max log MAP algorithm
- Scaling of APPs
- Simultaneous decoding
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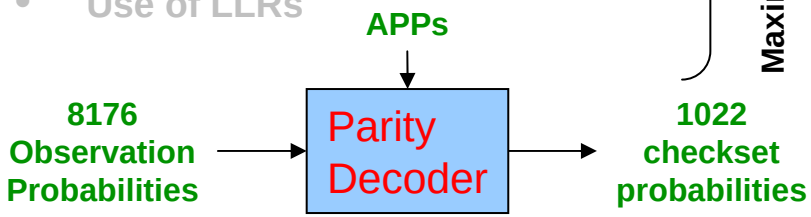
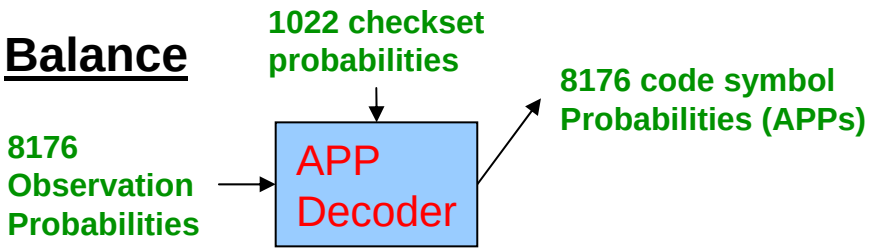
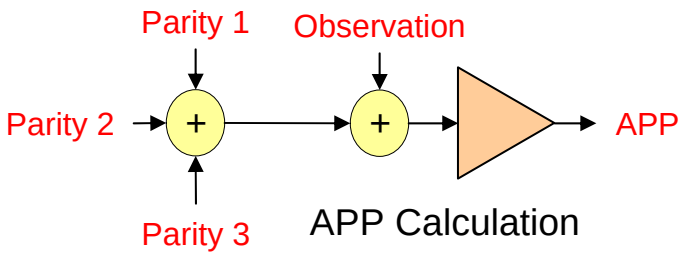
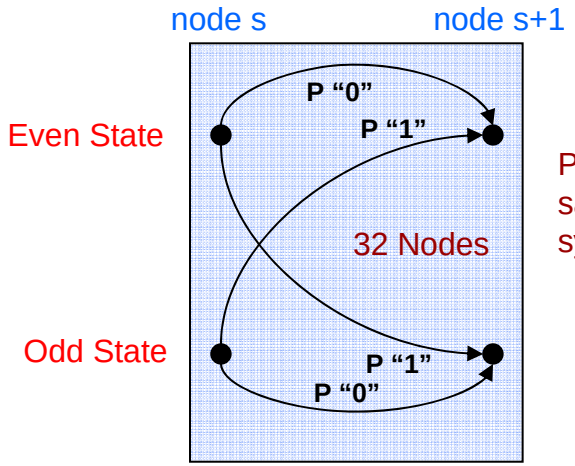
Maximize Throughput



Balance

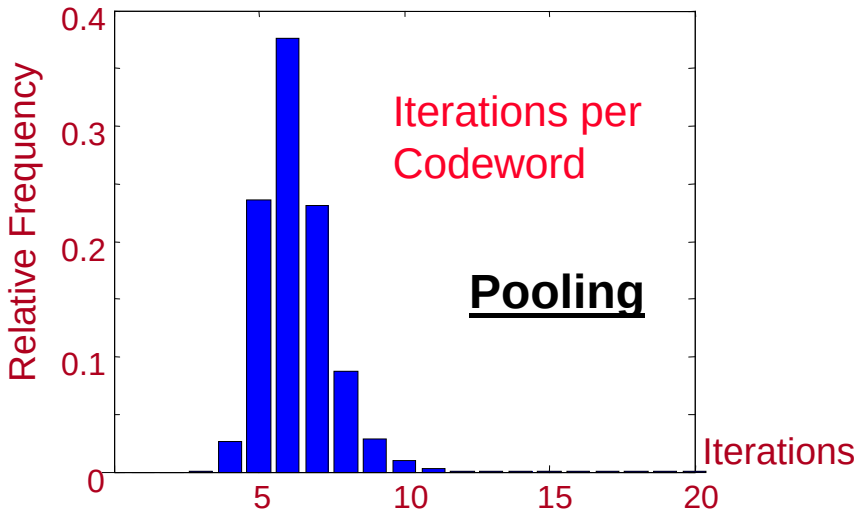






Prob checkset satisfied w/o code symbol i, i=0…8176

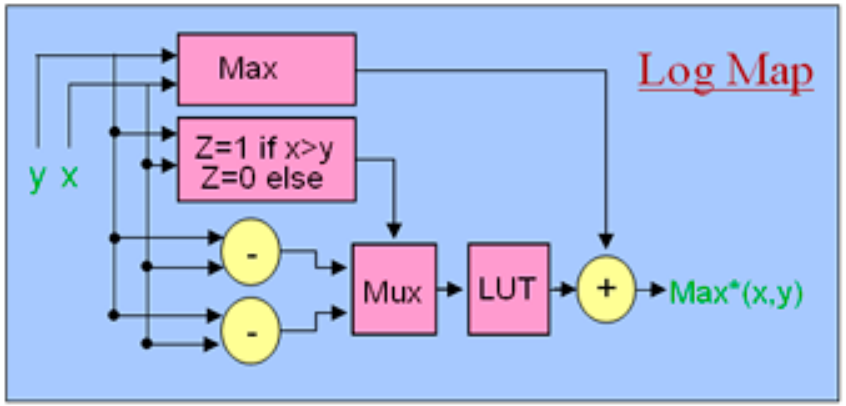
Slice of Parity Decoding Trellis

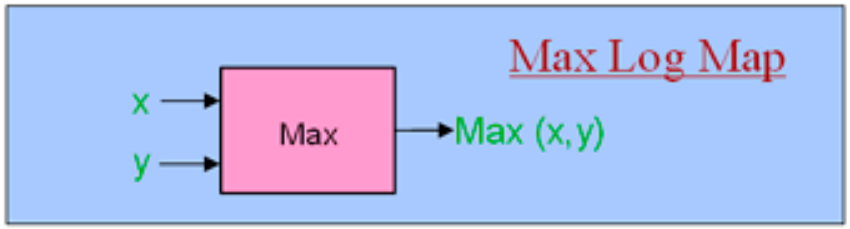


Turbo Decoding

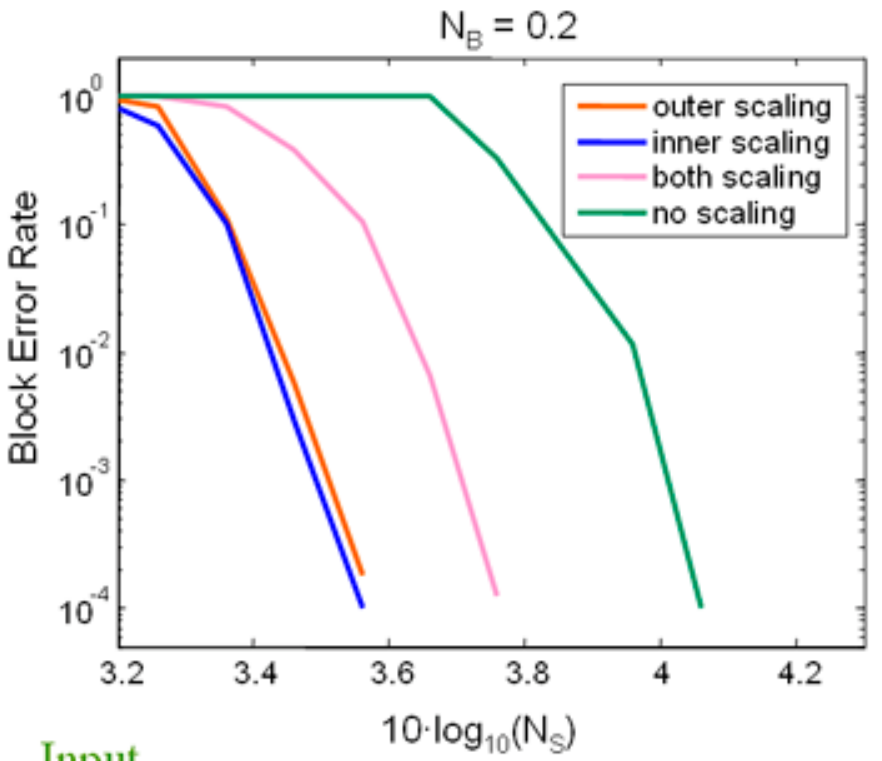
- Balance of component decoders
- Pooling
- **Max log MAP algorithm**
- **Scaling of APPs**
- Simultaneous decoding
- **Use of LLRs**

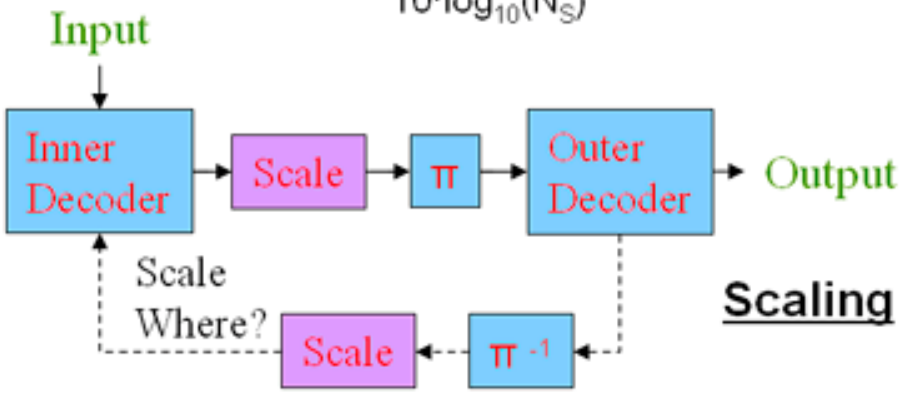
Maximize Throughput





Max Log Map





Scaling