

A New Class of High Performance FFTs

Dr. J. Greg Nash
Centar (www.centar.net)
jgregnash@centar.net

**High Performance Embedded Computing (HPEC)
Workshop**

19-21 September 2006

Comparative Features

- Transform size N not restricted to powers of two
- Circuit is scalable
- Uses block floating point and floating point
- Higher throughput
- Low computational latency
- Based on small, simple PE (adder), locally connected
- 1-D or 2-D transforms

Performance Comparison: 256-point DFT

Category	Altera	Base-4
Throughput (cycles/DFT)	256	240
Clock speed (MHz)	302	363
Throughput (μsec)	0.85	0.67
Signal/Noise (db)	86.9	89.0
Total ALUTs	7555	7790
18-bit multipliers	12	16

