Improving the Performance of Parallel Backprojection on a Reconfigurable Supercomputer

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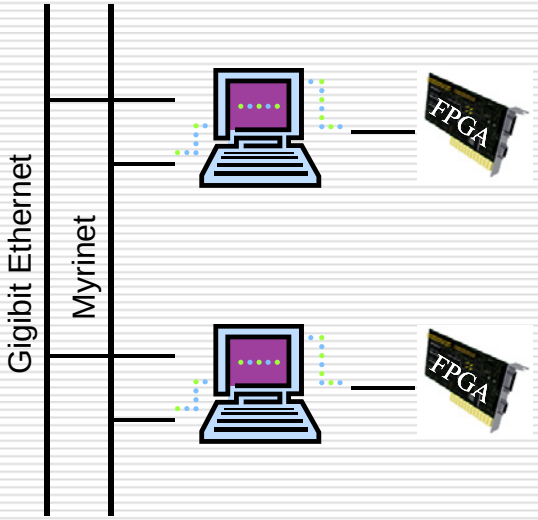
Exploitable Parallelism

- HHPC at AFRL in Rome: 48-node supercomputer with FPGAs
  - 2x 2.2GHz Xeon CPUs
  - Wildstar II/PCI FPGA board
- HPEC'05: 32-node version of backprojection using FPGAs
  - 26x speedup over single-node software-only
- Bottlenecks to performance:
  - Slow clustered filesystem
  - Data transfer times (CPU-to-FPGA) dominated processing time



Successful Performance Tuning

- Single-node (with FPGA) performance increased approximately 2.5x over previous results
  - Improved CPU-to-FPGA data transfer
  - FPGA masters entire process
  - Increased exploitation of fine-grained parallelism
- Additional ~20x improvement due to system architecture
  - Removed filesystem dependency
  - Improved data distribution model
- When applied to 32-node clustered application, 500-600x speedup over single-node software projected
- Details available on the poster!