Design of Path Optimization Algorithm Using COTS FPGA Hardware and Software Platforms

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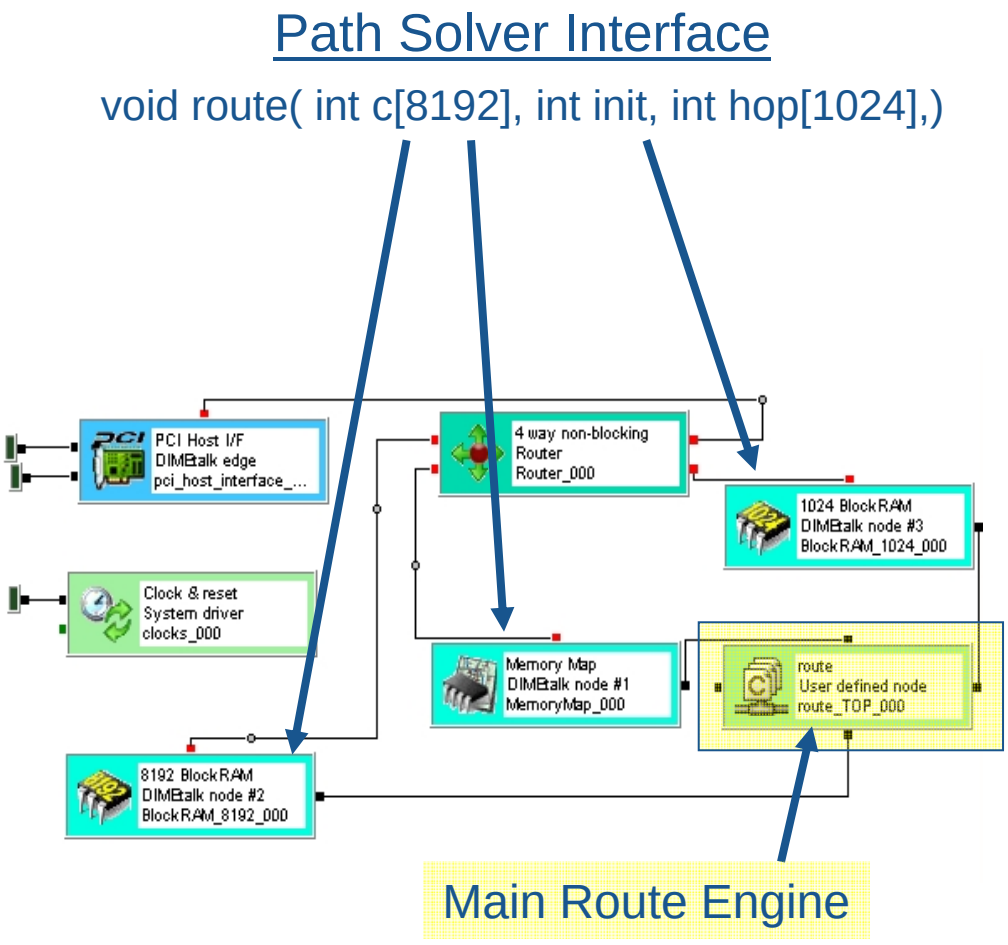
Path Optimization Algorithms

- Graph-based path optimization are applicable in a variety of areas
  - Latency critical computation in reactive path planning
  - Expensive component of place and route
  - Hidden Markov Model for Speech Processing
  - Communications error correction
- Shortest Path Algorithm Implementation
  - Generalizable dynamic programming engine
  - Interfaced as computation server
    - Persistent data initialization
    - Instance specific run control



Path Optimization Design Results

- Five-million "equivalent gate" design on a Xilinx Virtex-II 2V4000 running at 100MHz
- Mixed memory, processing, and logic
  - 27 x 1K X 32-bit dual port memories
  - 336 operators (including lower bit-widths)
  - The first pass design outperforms modern conventional processors by 10-to-1 in actual time
  - 100-to-1 performance improvement in cycle count
- Substantially enhanced performance
  - Higher levels of unrolling
  - Close to 100-fold improvements in performance
  - No custom timing optimization
- Full design productivity
  - Took approximately one person-month
  - Estimated time of 1 year to perform the same tasks using low level hardware description language