



FPGA Technology Meeting the Multicomputer Environment: Improving Processing Performance and Bandwidth in Advanced Naval Radar Missions

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Naval Missions of the Future



- **Aegis Weapons System** provides heart of surveillance and airborne threat response for the U.S. Navy
 - Incorporates advanced radar systems with Mercury Computer Systems' signal processing systems
- **Lockheed Martin extends traditional surveillance and response to include sea-based Ballistic Missile Defense (BMD) capability**
 - Requires real-time detection, tracking, and discrimination performance against threat-representative targets and countermeasures
- **Combined goal of Lockheed Martin & Mercury to architect multi-mission capable solution**
 - Need for system architectures with a mixture of GPPs and FPGAs to satisfy processing needs
 - Rich in flexible and reconfigurable resources
 - Offering unprecedented I/O bandwidth

Mission-critical demands for tomorrow's naval threats require ever increasing application enrichment and system performance

Mission Goals Set FCN Requirements

- **Integration of FPGA module into PowerStream 7000 delivered more system performance**

- Input high-bandwidth raw data from a remote sensor
- Perform front-end algorithms in real-time
- Handle diverse set of processing scenarios
- Distribute post-processed data to a GPP array

- **Mission requirements for FCN module**

- Utilize standardize COTS interfaces for sensor I/O, control, and data
- Allow high-bandwidth/low-latency communication between FPGAs in system
- Support fault detection in the design
- Provide a significantly dense board that offers the flexibility to power more than one mission application
 - Large FPGAs with a significant amount of gates for application development
 - Support high-bandwidth external RAM for memory- intensive algorithms
 - Support for commercially available FPGA development tools
- Enable FPGA-mastered DMA capability for sending/receiving data from/to GPP array
- Allow for fast download of FPGA bit streams to support low-latency mission changes



FCN Architecture

- **Three FPGA node architecture**
 - Each node - 32 MB QDR SRAM
 - Each node -128 MB RLD RAM
- **Two 10 Gigabit Ethernet ports for standardized, high-speed I/O**
- **Tremendous chip-to-chip interconnect for on-board data distribution**
 - Five MGTs at 2.5 Gbps between each FPGA
- **Parallel RapidIO interconnect at 622 MB/sec peak per link**

