Radar Digital Beam-Former Utilizing FPGA Based COTS Processors

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ABSTRACT

A real time Radar Digital Beam-Former Front End presents a challenging HPEC application. The Radar digital beam-former requires significant input bandwidth and data distribution complexity along with Front End Filter Processing loads that stress most advanced embedded computing platforms. Lockheed Martin has implemented a demonstration system to perform Real Time Digital Beam-Former Front End functions to serve as a risk reduction activity for a Digital Array Radar.

The Front End processing includes sensor interface receive processing, digital filtering and digital beam-forming. As part of an open architecture strategy for the Digital Front End a standard interconnect to the receiver subsystem incorporated a sensor interface utilizing the 10 Gbit Ethernet interface. The digital filter functions follow the interface processing and include digital product detection, interpolation, decimation, channel equalization and frequency offset processing. The filtering functions will operate with input sample rates of up to 200 MHz per input channel and output sample rates of 60, 20, and 5 MHz per output channel. Following the digital filter functions the I/Q results are processed by the beam-former to develop up to 16 simultaneous arbitrarily weighted combinations of the input channel data. The beam-former output data is supplied to a DSP subsystem for subsequent pulse compression and detection processing. The Digital Front End provides high speed data recording of A/D samples, I/Q data or Formed Beams to assess system capabilities and to facilitate system integration and test.

This paper will present the implementation and testing of this Radar Digital Beam-Former Front End. We will address the network and interconnect architecture developed to support a scalable number of input channels of the beam-former and the distribution of high bandwidth beam interfaces to the DSP. An overview of the FPGA partitioning and technology utilized to perform digital filtering and beam-forming as well as strategies utilized for software control, system synchronization, fault recovery and testing will be described. In summary an overview of the Real Time Digital Front End performance results, lessons learned and future challenges are presented

Digital Front End Description

The Digital Beam-Former Front End hardware consists of a Mercury PowerStream 7000 multiprocessor computer composed of a hybrid of FPGA processors and PowerPC processor modules and a VMETRO Memory Data Recorder. System interconnects include 10Gbit interfaces for sensor channel inputs. After the landing of the sensor data within FPGA processing nodes, filtering and bandwidth reduction is performed. Following the filtering functions within each FPGA processing node a complex weighted sum of the associated input channels are created to start the beam-forming process. A summation is performed by transferring the weighted results across each of the FPGA processing nodes with each element contributing the weighted sum of the channels in which it is connected. The partial sums are then flowed through all the FPGA processing nodes until all beam contributors are weighted and summed. This summing function is performed over multiple FPGA devices interconnected through the Xilinx RocketIO interfaces directly on the FPGA processing nodes. This approach reduces the impact of the intense I/O bandwidth requirements of beam-forming from the remainder of the processing system.

Following the completion of the combining of all filtered sensor channels the data is queued within the final stage FPGA nodes. Final beam-formed data is transferred from the data queues within the FPGA processing nodes via the RapidIO network within the PowerStream 7000.

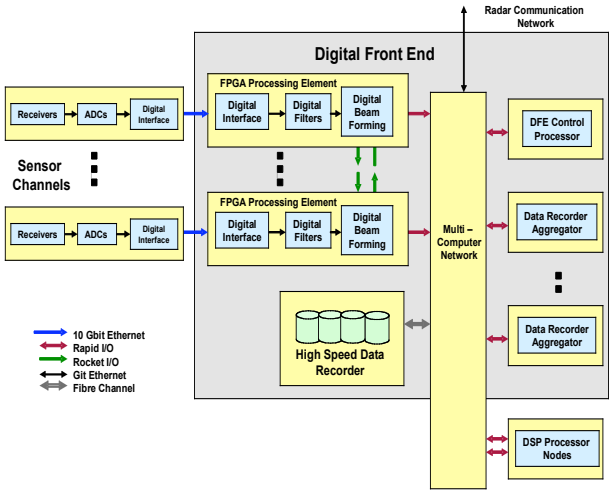

Figure 1: Digital Front End Functional Diagram

The Digital Front End (DFE) Control Processor and the Data Recorder Aggregator hardware is a Mercury PowerPC-based computer node which includes a PowerPC, memory and interconnects to the multi-computer fabric. Each PowerStream Processor Module contains five PowerPC7447 G4 processors with interfaces to the RapidIO fabric. The DFE Control processor performs

initialization, Radar command parsing, command distribution to the FPGA processing nodes, and overall status collection. The role of the data recorder aggregator is to collect the data from the record buffers within the individual FPGA processing nodes and format the data for delivery to the VMETRO high speed data recorder.

FPGA Design

Multi-rate digital filtering allows sampling to occur at the rate of the highest performance A/D's, easing RF filter requirements without compromising base-band selectivity. Poly-phase filtering techniques enable an efficient FPGA implementation balancing the demands on logic, routing, and dedicated multipliers within the target device.

Various techniques exist for implementing filters in FPGA devices. Dedicated resources such as Block RAM and "shift register logic" were used to phase coefficients and move data in a compact manner to gain highly efficiency utilization of the arithmetic resources and to conserve routing resources.

Filter performance was enhanced by effectively extending precision (coefficient range) with selective filter taps. This technique efficiently extended the performance for the filter structures without the need to perform full floating point arithmetic.

Multigigabit transceivers provide the capacity to carry individual channels through the filtering stages and then across the channels to sum their weighted contributions.

Summary

Our approach exploits recent technological advances in several areas to achieve high performance. A multi-computer platform was selected to provide high density heterogonous processing nodes with a high bandwidth network interconnect structure. FPGA technology was utilized to achieve high operational density in areas where regular structures dominate, such as front end filters. Local high bandwidth domain specific interconnect are leveraged to support the local communications requirements of beam-forming.

Within this paper several key areas of the Digital Beam-Former design, development and testing will be chronicled. A summary of the Digital Front End is provided with requirements and implementation architecture. An overview of Lockheed Martin's rapid prototype implementation strategy with key embedded equipment suppliers will be discussed. The functional mapping of the Real Time Digital Beam Former problem including processing and I/O is described. The control software architecture utilized to provide command and status information to the processing nodes and direct data distribution to the DSP subsystem is reviewed. Strategies and approaches are described that support synchronization of the multiple input channels and communication paths and the detection and recovery from communication faults. The experience and strategies utilized during integration and test of the digital front end and what design features were utilized during the testing process. Integration and test results of the Digital Front End will be provided including throughput.

In summary the results along with lessons learned about the Lockheed Martin Radar Digital Beam-Former demonstrator are described. An overview of the design, performance, and issues encountered during the development and testing will be included. An analysis of this Beam-Former application and related future challenges are presented to the HPEC community.