Real-Time Adaptive Signal Processing Development for US Navy Torpedoes

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Overview

The US Navy torpedo development effort aims to extend the effectiveness of the Mk 48 and Mk 54 torpedoes. MIT Lincoln Laboratory (MIT/LL) is involved with the Navy in developing algorithms to improve current torpedo performance, processor hardware architectures to accommodate present and projected torpedo algorithms, and initial operating capability software that can accommodate future growth over the processor's life cycle. In the past, hardware architectures had limited processing capability with low computational throughput [1]. Today's computational thresholds, however, are less of a concern in torpedo systems. Empty hardware slots and faster processors in the current torpedoes allow for upgrades, providing developers with the potential to implement higher-performance algorithms with greater computational complexity.

To improve current torpedo performance, MIT/LL has developed a torpedo adaptive signal processing (TASP) stream and performed a complexity analysis for this application. For a real-time demonstration of TASP, MIT/LL has selected hardware relevant to the Mk 48 and Mk 54 torpedoes [2,3], and derived a methodology to facilitate development of the TASP stream on the target architecture.

Adaptive signal processing

The current signal processing baseline for the Mk 48 and Mk 54 torpedoes involves conventional beamforming, conventional sidelobe blanking, and split-beam angle estimation. This method performs well in white noise; however, it may perform sub-optimally in the presence of interferers (i.e. countermeasures).

In conjunction with the Naval Undersea Warfare Center (NUWC) in Newport, RI, MIT/LL has developed TASP in an effort to increase torpedo effectiveness in shallow water (littoral) environments. TASP consists of three principal kernels: adaptive beamforming, adaptive side-lobe blanking, and adaptive angle estimation. TASP improves torpedo performance in the presence of countermeasures by adapting to the data and by canceling interference. Unfortunately, TASP is computationally expensive, requiring eight times the number of floating point operations (flops) as the baseline processor. Variants of the TASP kernels have been implemented to minimize computational complexity without significantly compromising torpedo effectiveness. Fig. 1 compares the computational complexity of two different adaptive beamforming kernels: the "original" algorithm and a modified version using "weight sharing" to reduce the processing load.

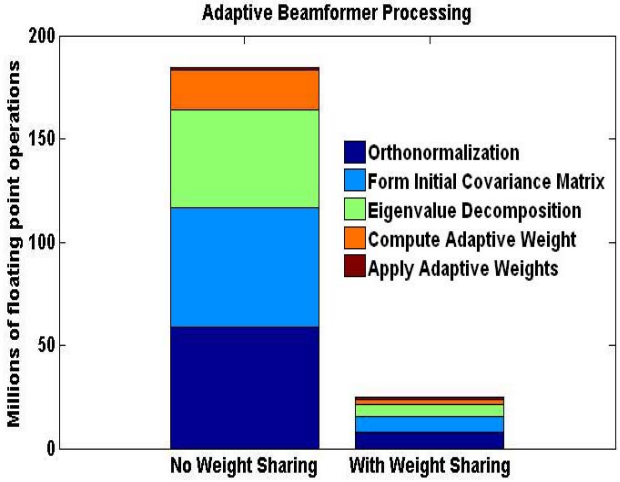

Figure 1 – Parallel FFT Software Performance

System performance

To quantify computational performance, MIT/LL has performed a complexity analysis of the adaptive signal processing stream. This consists of deriving formulas that estimate, as a function of run-time parameters, the total number of flops required by TASP. These formulas have been verified and embedded into the Matlab signal processing stream. By embedding the complexity formulas, MIT/LL can automate system performance analysis with the use of the Performance Analysis Simulator (PAS), for which the user interface is shown in Fig. 2. PAS allows the operator to select from multiple hardware/software configurations, plot results from various kernels of TASP, and evaluate computational performance to optimize bottlenecks and enable real-time processing.

Hardware technology

MIT/LL has established a "torpedo advanced processor build" (TAPB) Laboratory. One objective of this lab is to replicate aspects of the torpedo's real-time hardware, so that new algorithms can be tested and their performance measured. For the actual torpedo hardware, Raytheon has chosen the Radstone G4DSP quad 400 MHz Power PC (PPC) as its commercial off the shelf (COTS) equipment for the signal processing card. MIT/LL has chosen to purchase the next-generation card (G4DSP-XE quad 1 GHz PPC), thus allowing MIT/LL to provide an advance indication of possible benefits the Navy may realize in the next "hardware refresh" cycle.

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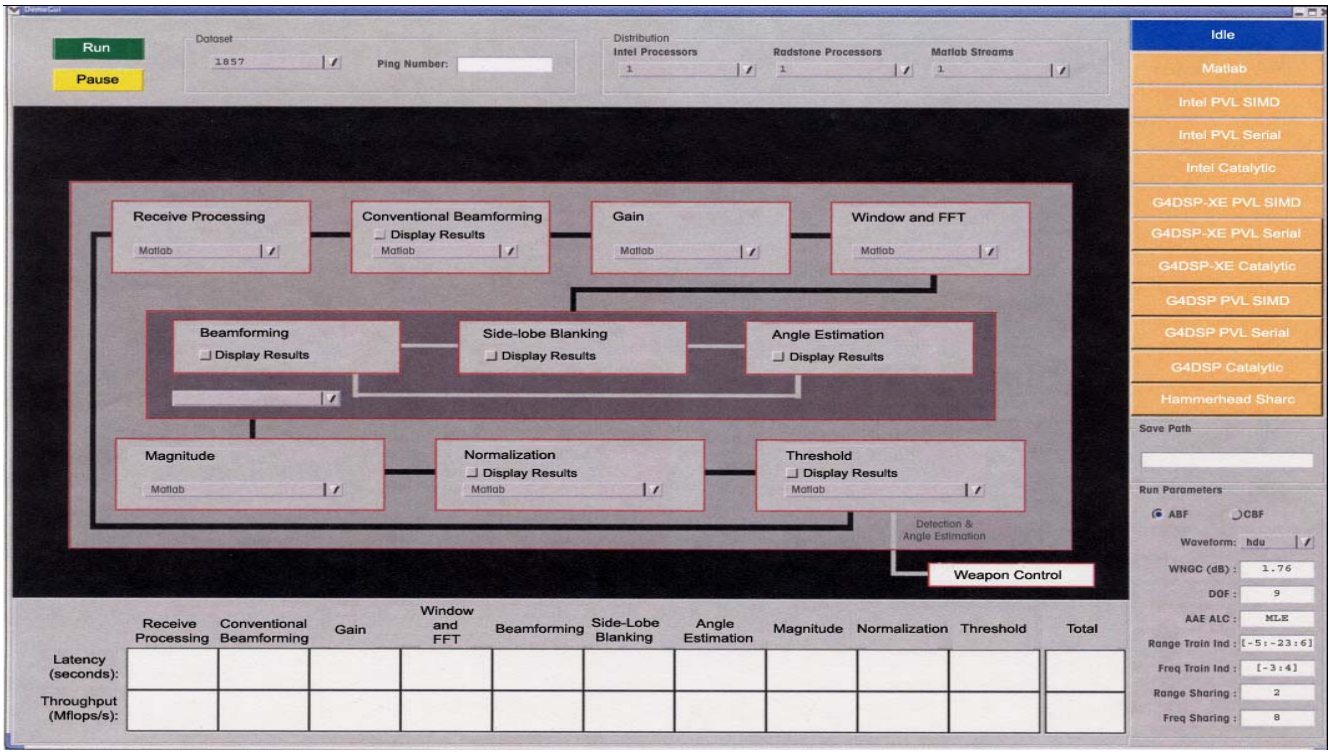

Figure 2 – Performance Analysis Simulator (PAS) User Interface

Development methodology

MIT/LL has utilized an advanced methodology to expedite real-time development of TASP. This methodology allows an algorithm developer to see how TASP progresses from single processor (serial) Matlab code all the way through multiple processor (parallel) C/C++ code. The development methodology also exploits various hardware architectures such as a single node Intel processor and the target real-time embedded parallel processor (i.e., the G4DSP-XE). The final objective is to produce parallel C/C++ code that operates in real-time on the target platform. This methodology is summarized in Fig. 3.

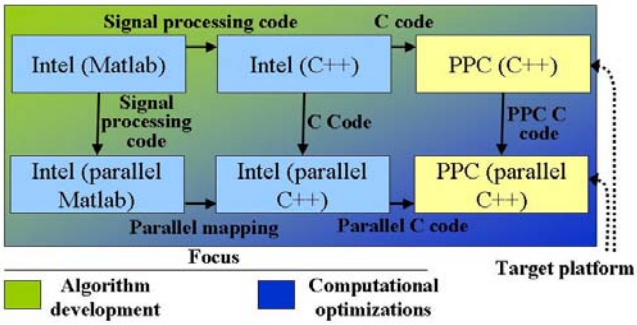

Figure 3– Parallel FFT Software Performance

Summary

MIT/LL and NUWC have collaborated to develop an adaptive signal processing stream for the Mk 48 and Mk 54 torpedoes. To analyze and optimize this processing stream, MIT/LL has purchased embedded signal processing boards similar to those found in the actual torpedoes. Complexity analysis formulas predict the number of flops the signal processing stream requires, allowing automated system performance analysis of the individual kernels. MIT/LL support for torpedo development has therefore resulted in a stronger "integrated product team" to help both government and industry design better products for the Navy.

References

[1] Committee for Undersea Weapons Science and Technology Naval Studies Board. *An Assessment of Undersea Weapons Science and Technology*. National Academy of Sciences, 2000.

[2] Raytheon Company. *MK 48 ADCAP Mod 6 Advanced Technology data sheet*, 2003.

[3] Radstone Technology. *Radstone Technology Announces a New Torpedo Contract from Raytheon*, Radstone Technology News, March 2004.