NMP ST8 High Performance Dependable Multiprocessor

10th High Performance Embedded Computing Workshop
@ M.I.T. Lincoln Laboratory

September 20, 2006

Dr. John R. Samson, Jr.
Honeywell Defense & Space Systems, Clearwater, Florida

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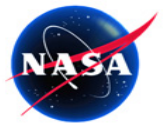

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Outline

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- Introduction
  - Dependable Multiprocessing technology
    - overview
    - hardware architecture
    - software architecture
- Current Status & Future Plans
- TRL5 Technology Validation
  - TRL5 experiment/demonstration overview
  - TRL 5 HW/SW baseline
  - key TRL5 results
- Flight Experiment
- Summary & Conclusion
- Acknowledgements
- References

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DM Technology Advance: Overview

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- **A high-performance, COTS-based, fault tolerant cluster onboard processing system that can operate in a natural space radiation environment**
  - **high throughput, low power, scalable, & fully programmable (>300 MOPS/watt)**
  - **technology independent system software that manages cluster of high performance COTS processing elements**
  - **technology independent system software that enhances radiation upset immunity**
  - **high system availability (>0.995)**
  - **high system reliability for timely and correct delivery of data (>0.995)**

Benefits to future users if DM experiment is successful:

- 10X – 100X more delivered computational throughput in space than currently available
- enables heretofore unrealizable levels of science data and autonomy processing
- faster, more efficient applications software development
  - -- robust, COTS-derived, fault tolerant cluster processing
  - -- port applications directly from laboratory to space environment
    - --- MPI-based middleware
    - --- compatible with standard cluster processing application software including existing parallel processing libraries
- minimizes non-recurring development time and cost for future missions
- highly efficient, flexible, and portable SW fault tolerant approach applicable to space and other harsh environments, including large (1000-node) ground-based clusters
- DM technology directly portable to future advances in hardware and software technology

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DM Technology Advance: Key Elements

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- **A spacecraft onboard payload data processing system architecture, including a software framework and set of fault tolerance techniques, which provides:**

  A. **An architecture and methodology that enables COTS-based, high performance, scalable, multi-computer systems, incorporating co-processors, and supporting parallel/distributed processing for science codes, that accommodates future COTS parts/standards through upgrades**

  B. **An application software development and runtime environment that is familiar to science application developers, and facilitates porting of applications from the laboratory to the spacecraft payload data processor**

  C. **An autonomous controller for fault tolerance configuration, responsive to environment, application criticality and system mode, that maintains required dependability and availability while optimizing resource utilization and system efficiency**

  D. **Methods and tools which allow the prediction of the system's behavior across various space environments, including: predictions of availability, dependability, fault rates/types, and system level performance**

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Dependable Multiprocessor: The Problem Statement

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- **Desire - -> ‘Fly high performance COTS multiprocessors in space’**
  - **Problems:**
    - **Single Event Upset (SEU) Problem: Radiation induces transient faults in COTS hardware causing erratic performance and confusing COTS software ***
      - the problem worsens as IC technology advances and inherent fault modes of multiprocessing are considered
      - no large-scale, robust, fault tolerant cluster processors exist
    - **Cooling Problem: Air flow is generally used to cool high performance COTS multiprocessors, but there is no air in space**
    - **Power Efficiency Problem: COTS only employs power efficiency for compact mobile computing, not for scalable multiprocessing systems but, in space, power is severely constrained – even for multiprocessing**

To satisfy the long-held desire to put the power of today’s PCs and supercomputers in space, three key problems, SEUs, cooling, & power efficiency, need to be overcome

* As advanced semiconductor technologies become more susceptible to soft faults due to increased noise, low signal levels, and terrestrial neutron activity DM technology is equally applicable to terrestrial applications, e.g., UAVs.

Dependable Multiprocessor: The Solution

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- **Desire - - ‘Fly high performance COTS multiprocessors in space’**
  - **Solutions:**
    - **Single Event Upset (SEU) Problem Solution (aggregate):**
      - **Efficient, scalable, fault tolerant cluster management**
      - **Revise/embellish COTS Sys SW for more agile transient fault recoveries**
      - **Revise/embellish COTS Sys SW to activate transient fault detects & responses**
      - **Create Applications Services (API’s) which facilitate shared detection and response between App’s & Sys SW for accurate, low overhead fault transient handling**
      - **Replace SEU/latch-up prone, non-throughput impacting COTS parts with less prone parts**
      - **Model SEU transient fault effects for predictable multiprocessor performance**
    - **Cooling Problem Solution:**
      - **Mine niche COTS aircraft/industrial conductive-cooled market, or upgrade convective COTS boards with heat-sink overlays and edge-wedge tie-ins**
    - **Power Efficiency Problem Solution:**
      - **Hybridize by mating COTS multiprocessing SW with power efficient mobile market COTS HW components**

ST8 Dependable Multiprocessor technology solves the three problems which, to date, have prohibited the flying of high performance COTS multiprocessors in space

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DM Hardware Architecture

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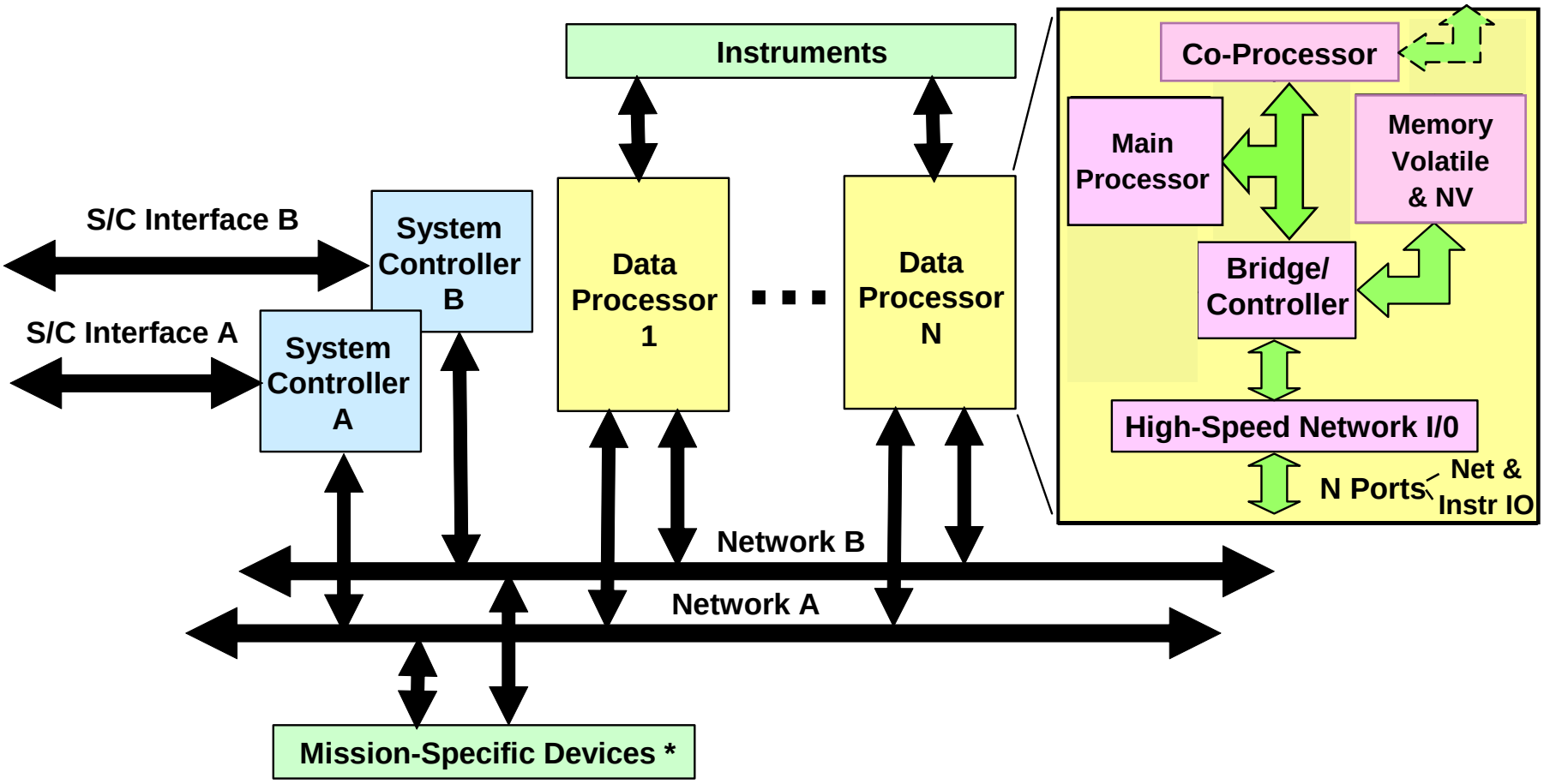

* Mass Data Storage Unit, Custom Spacecraft I/O, etc.

Addresses Technology Advance components A, B, and C

DM Software Architecture

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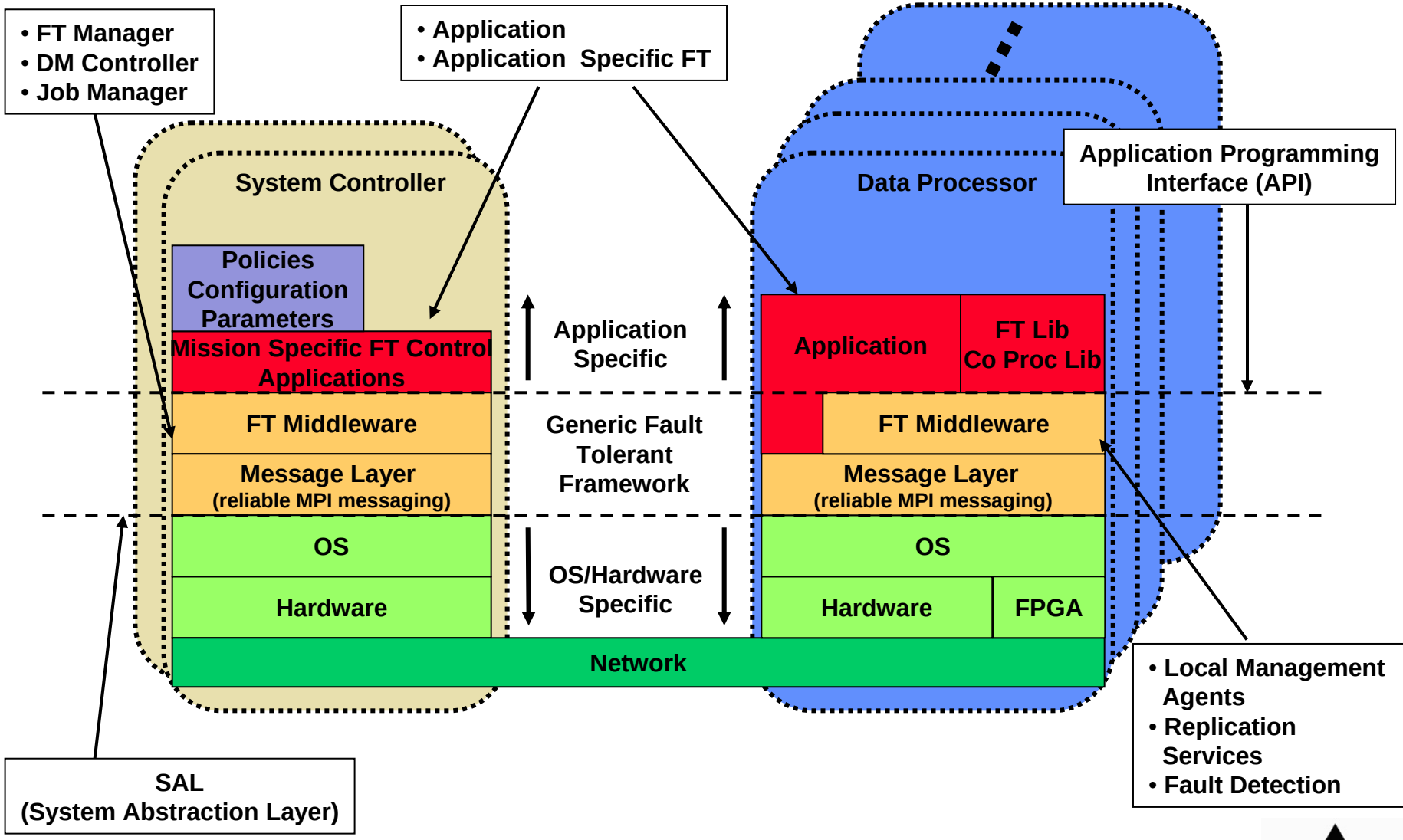

Addresses Technology Advance components A, B, and C

DM Software Architecture "Stack"

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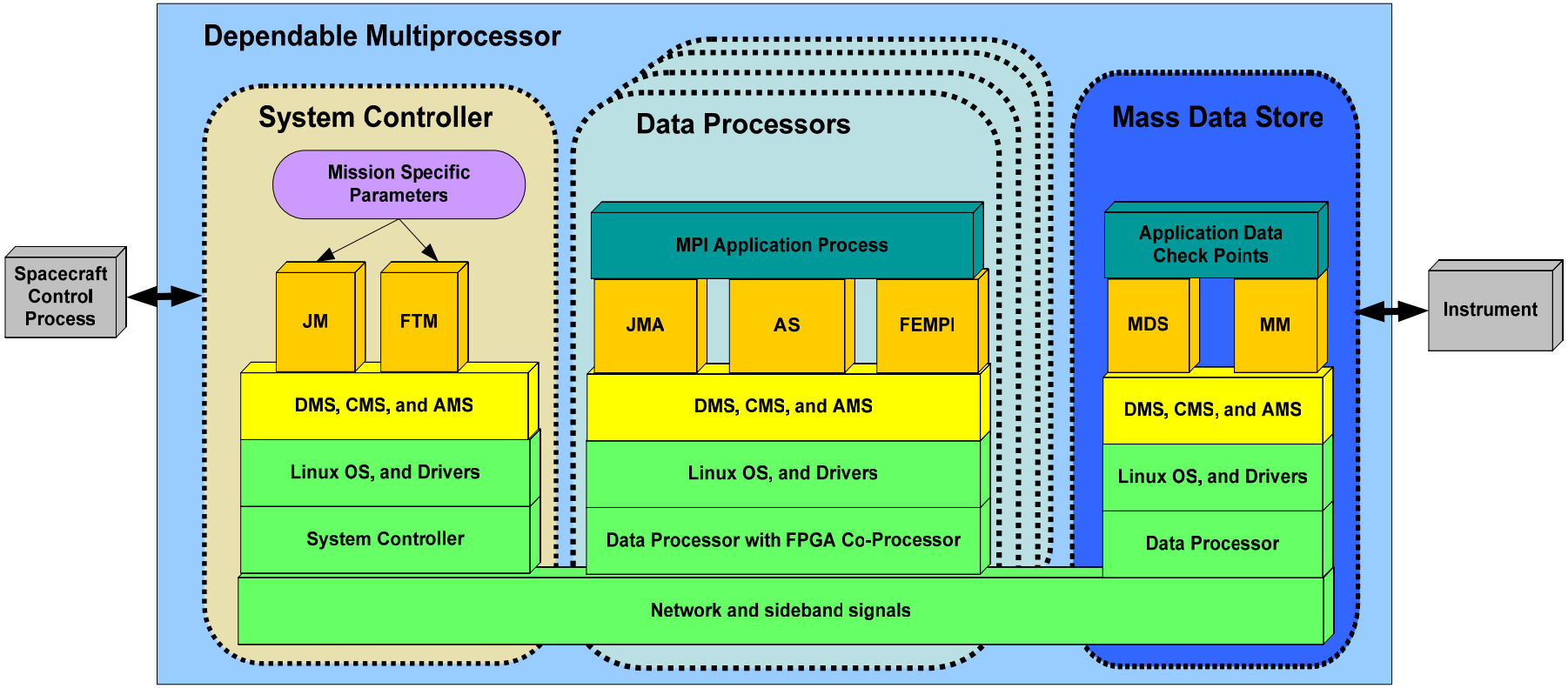

- Mission Specific Components
- Dependable Multiprocessor Specific Components
- HA Middleware
- Platform Components
- Application Components

JM – Job Manager
JMA – Job Manager Agent
MM - Mission Manager
FTM- Fault Tolerance Manager
FEMPI – Fault Tolerant Embedded Message Passing Interface

AS – Application Services
MDS – Mass Data Storage
CMS – Cluster Management Services
AMS – Availability Management Services
DMS – Distributed Messaging Services

Addresses Technology Advance components A, B, and C

[FPGA?]

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Examples: User-Selectable Fault Tolerance Modes

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Fault Tolerance Option	Comments
NMR Spatial Replication Services	Multi-node HW SCP and Multi-node HW TMR
NMR Temporal Replication Services	Multiple execution SW SCP and Multiple Execution SW TMR in same node with protected voting
ABFT	Existing or user-defined algorithm; can either detector detect or detect and correct data errors with less overhead than NMR solution
ABFT with partial Replication Services	Optimal mix of ABFT to handle data errors and Replication Services for critical control flow functions
Check-pointing Roll Back	User can specify one or more check-points within the application, including the ability to roll all the way back to the original
Roll forward	As defined by user
Soft Node Reset	DM system supports soft node reset
Hard Node Reset	DM system supports hard node reset
Fast kernel OS reload	Future DM system will support faster OS re-load for faster recovery
Partial re-load of System Controller/Bridge Chip configuration and control registers	Faster recovery that complete re-load of all registers in the device
Complete System re-boot	System can be designed with defined interaction with the S/C; TBD missing heartbeats will cause the S/C to cycle power

Dependable Multiprocessor
Benefits - Comparison to Current Capability

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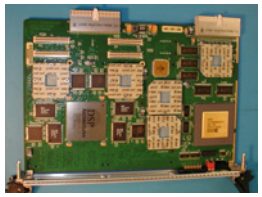
NMP EO3 Geosynchronous Imaging Fourier Transform Spectrometer Technology Indian Ocean Meteorological Instrument (IOMI) - NRL

Radiation Tolerant 750 PPC SBC		133 MHz ~ 266 MFLOPS ~ 1.2 kg	1K Complex FFT in ~ 448 μsec ~ 13 MFLOPS/watt
Radiation Hardened Vector Processor		DSP24 @ 50 MHz ~ 1000 MFLOPS ~ 1.0 kg	1K Complex FFT in ~ 52 μsec ~45 MFLOPS/watt

NMP ST8 Dependable Multiprocessor Technology

7447a PPC SBC with AltiVec		800 MHz ~ 5200 MFLOPS ~ 0.6 kg	1K Complex FFT in ~ 9.8 μsec ~ 433 MFLOPS/watt

The Rad Tolerant 750 PPC SBC and RHVP shown are single board computers without the power penalty of a high speed interconnect. The power density for a DM 7447a board includes the three (3) Gigabit Ethernet ports for high speed networking of a cluster of these high performance data processing nodes. The ST8 technology validation flight experiment will fly a 4-node cluster with a Rad Hard SBC host.

DM technology offers the requisite 10x – 100x improvement in throughput density over current spaceborne processing capability

DM Technology Readiness & Experiment Development Status and Future Plans

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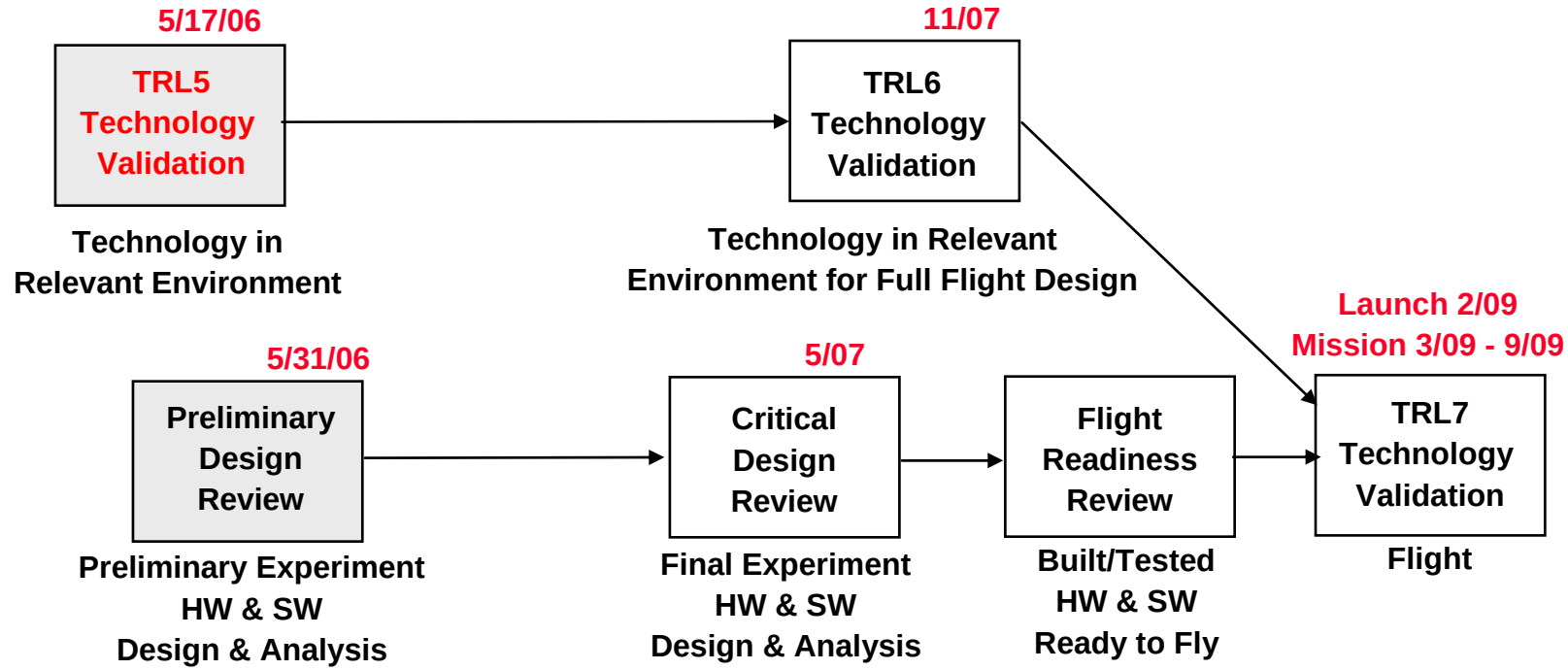

5/5/06 & 5/16/06

Preliminary Radiation Testing

Critical Component Survivability & Preliminary Rates

Final Radiation Testing

Complete Component & System-Level Beam Tests

Test results indicate critical μP & host bridge components will survive and upset adequately @ 320 km x1300 km x 98.5° orbit

Key: - Complete

TRL 5 Technology Validation Overview

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- Implemented, tested, and demonstrated all DM functional elements
- Ran comprehensive fault injection campaigns using NFTAPE * tool to validate DM technology
- Injected thousands of faults into the instrumented DM TRL5 testbed
- Profiled the DM TRL5 testbed system
- Collected statistics on DM system response to fault injections
- Populated parameters in Availability, Reliability, and Performance Models
- Demonstrated Availability, Reliability, and Performance Models
- Demonstrated 34 mission "application" segments which were used to exercise all of the fault tolerance capabilities of the DM system
- Demonstrated scalability to large cluster networks
- Demonstrated portability of SW between PPC and Pentium-based processing systems

* NFTAPE - Network Fault Tolerance and Performance Evaluation tool developed by the University of Illinois and Armored Computing Inc.

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Analytical Models

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- **Developed Four Predictive Models**
  - **Hardware SEU Susceptibility Model**
    - Maps radiation environment data to expected component SEU rates
    - Source data is radiation beam test data
  - **Availability Model**
    - Maps hardware SEU rates to system-level error rates
    - System-level error rates + error detection & recovery times ➔ Availability
    - Source data is measured testbed detection / recovery statistics
  - **Reliability Model**
    - Source data is the measured recovery coverage from testbed experiments
  - **Performance Model**
    - Based on computational operations, arithmetic precision, measured execution time, measured power, measured OS and DM SW overhead, frame-based duty cycle, algorithm/architecture coupling efficiency, network- level parallelization efficiency, and system Availability
    - Source data is measured testbed performance and output of the Availability model predictions

Addresses Technology Advance component D

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TRL5 Testbed

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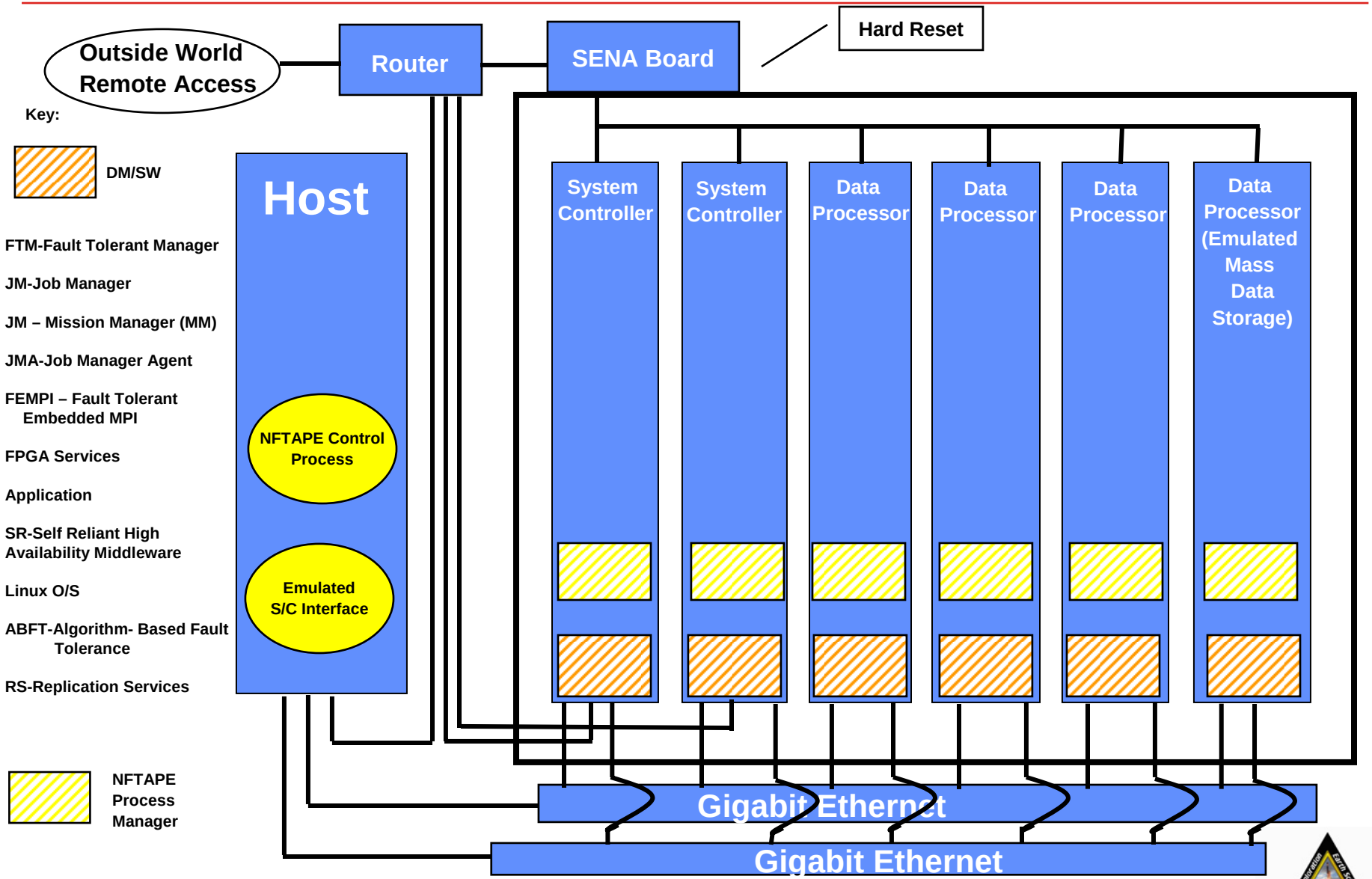

Automated Process of Injecting Errors Using NFTAPE

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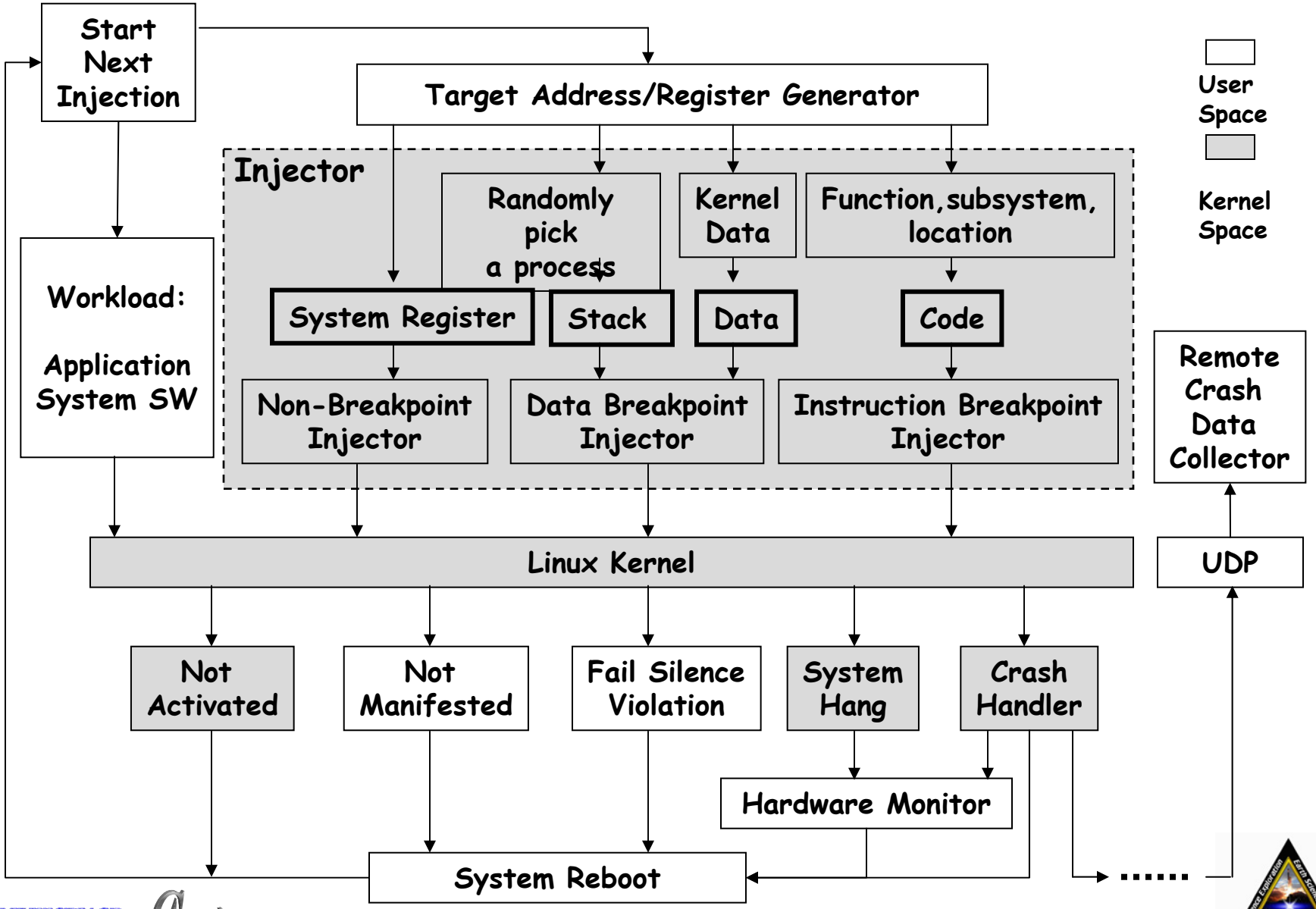

NFTAPE Support for Error Injection into Processor Units

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Processor Functions	Direct injections	Emulation of fault effect
(1) L2 Cache (ECE protected in 7448)	L2CR (L2 cache control register; enabling parity checking, setting cache size, and flushing the cache) TLBMISS register used by TLB (translation lookaside buffer) miss exception handlers	Injections to instructions/data emulate incorrect binaries to be loaded to the L2 cache
(2)&(3) Instruction and data cache; instruction and data MMU	LDSTCR (Load/store control register). SR (segment registers); IBAT&DBAT (Block-address translation) arrays SDR (sample data register; specifies base address of the page table used in virtual-to-physical address translation)	Injections to instructions/data emulate incorrect binaries to be loaded to the L1 cache (both instructions and data)
(4) Execution Unit	GPR (general purpose registers), FLP (floating point registers), VR (vector registers) FPCSR (FP status and control register) XER (overflows and carries for int. operations)	Injection to instructions: (i) corruption of operands can emulate errors in register renaming; (ii) corruption of load/store instructions can mimic errors in calculating effective address or load miss
(5) Instruction Unit (fetch, dispatch, branch prediction)	CTR (Count Register); LR(Link register); CR (condition register)	Injections to branch and function call instructions emulate control flow errors
(6) System Bus Interface	No visible registers	Injections to instructions/data emulate errors in load queues, bus control unit., and bus accumulator
(7) Miscellaneous system functions	MSR (machine state register; saved before an exception is taken); DEC (decrementer register), ICTC (instr. cache throttling control register); Exception handling: DAR (data address register), DSISR (DSI source register; data storage interrupt), SRR (save & restore registers), SPRG (provided for operating system use)	

Example: Injection Profiling Results

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Test conditions:
- **Application**
- **FT mode(s)**

System-Level Error Manifestations

Test Run ID	# Injections	Injection Mode	Injection Space	Injection Type	Injection Base	Injection Target	Application	FEMPI	ABFT on	RS on	# app crashes/ hangs	#JMA crashes/ hangs	#App Data errors	# SR failures	# DP switch-overs	# Network switch-overs	# Node crashes	#System crashes	#Golden Violations
May 11 14 55 10	100	Cumulative	User	Random	GPR	JMA	simpleLU	n	y	n	3	0	0	0	0	0	0	0	0
May 11 16 22 30	100	Cumulative	User	Random	GPR	simpleLU	simpleLU	n	y	n	3	6	0	1	0	0	0	0	0
May 12 07 34 20	100	Cumulative	User	Random	GPR	simpleLU	simpleLU	n	y	n	3	7	0	7	0	0	0	0	0
May 12 09 39 40	100	Cumulative	User	Random	CR	simpleLU	simpleLU	n	y	n	0	9	0	0	0	0	0	0	0
May 12 11 03 57	100	Cumulative	User	Random	FR	simpleLU	simpleLU	n	y	n	0	0	0	0	0	0	0	0	0
May 12 12 07 39	100	Cumulative	Kernel	Random	GPR	n/a	simpleLU	n	y	n	0	7	0	0	0	0	0	0	0
May 13 10 28 52	99	Cumulative	Kernel	Random	CR	n/a	simpleLU	n	y	n	6	1	0	0	0	0	0	0	0
May 13 14 25 49	100	Cumulative	User	Random	GPR	simpleLU	simpleLU	n	y	n	0	8	0	0	0	0	0	0	0
May 14 13 32 09	100	Cumulative	User	Random	TEXT	JMA	simpleLU	n	y	n	1	0	0	0	0	0	0	0	0
May 14 14 45 48	88	Cumulative	User	Random	TEXT	JMA	simpleLU	n	y	n	2	0	0	0	0	0	0	0	0
May 14 15 24 35	30	Cumulative	User	Random	DATA	JMA	simpleLU	n	y	n	1	0	0	0	0	0	0	0	0
May 14 15 43 05	15	Cumulative	User	Random	DATA	JMA	simpleLU	n	y	n	1	0	0	0	0	0	0	0	0
May 14 16 19 06	93	Cumulative	User	Random	DATA	simpleLU	simpleLU	n	y	n	0	0	0	0	0	0	1	0	0
May 14 18 28 16	51	Cumulative	User	Random	TEXT	srp	simpleLU	n	y	n	0	0	0	0	0	0	0	0	0
May 15 06 30 55	91	Cumulative	Kernel	Random	TEXT	n/a	simpleLU	n	y	n	0	0	0	14	0	0	1	0	0
May 15 08 19 11	30	Cumulative	User	Random	TEXT	srp	simpleLU	n	y	n	0	0	0	1	0	0	0	0	0
May 15 14 07 03	93	Single	User	Random	TEXT	JMA	simpleLU	n	y	n	0	2	0	0	0	0	0	0	0
May 15 14 44 14	73	Single	User	Random	TEXT	simpleLU	simpleLU	n	y	n	0	2	0	0	0	0	0	0	0
May 15 15 18 42	72	Cumulative	User	Random	TEXT	simpleLU	simpleLU	n	y	n	0	5	0	0	0	0	0	0	0
Total	1535								Total		20	47	0	23	0	0	2	0	0

Overall Measure of Coverage – the number of erroneous computations which exited the system without being detected – per definition of DM Reliability
- **erroneous outputs**
- **missed outputs (never completed/delivered)**

Example: Summary of Register Fault Injections & Fault Allocation to Processor Units

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Processor Functions	App/middleware failure [recovery]	Node failure [app. recovery]	Node failure [recovery; app. restart]	Total injections	Fault manifestation [%]
L2 Cache					
L2CR (L2 cache control reg)	0	0	0	19	
TLBMiss register	0	0	0	0	
L1 Instruction & data cache					
Instruction & data MMU					
LDSTCR	0	0	0	0	not writable
SR (segment registers)	1	4	11	282	
IBAT&DBAT arrays	0	8	4	256	
SDR (vitual to physical addr. trans.)	0	7	13	26	
Execution Unit					
GPR (general purpose)	37	1	0	583	
FLP, FPSCR (floating point)	0	0	0	208	
XER (overflows & carries)	0	0	0	106	
Instruction Unit					
CTR (count)	6	0	1	136	
LR (LNK - link)	4	0	10	144	
CR (CCR - condition)	1	0	2	108	
NIP (instruction pointer)	8	0	16	147	
System Bus Interface					
No visible registers					
Miscellaneous					
MSR (machine state)	2	1	7	116	
DEC(decrementer)	1	2	3	19	
HID (HW implementation reg)	0	1	0	40	
Exceptions (SPRG)	0	9	9	157	
PVR (CPU version reg)	0	0	0	18	
TBL, TBU (time base)	0	0	1	35	
ICTC (instr. cache throttling)	0	0	0	13	
TOTAL	**60**	**33**	**77**	**2413**	**7.045171985**
					7.05 +/- 1.02 %

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NMP Space Science Exploration Earth Science Exploration Breakthrough Technologies

Timing Instrumentation

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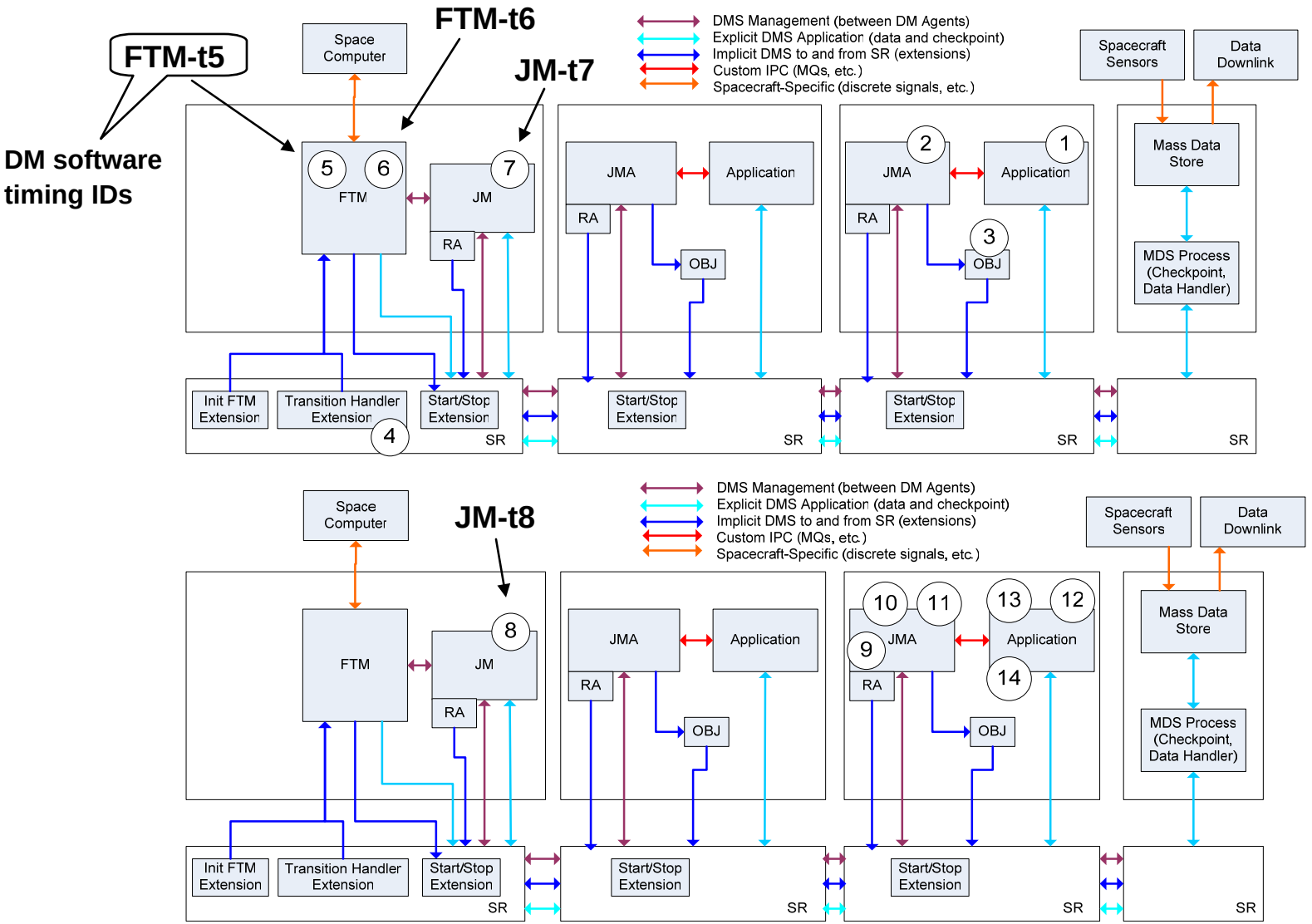

Example: DM Performance Statistics

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- **TRL5 testbed experiment timing data showing average measured values, maximum measured values, minimum measured values, and standard deviation of measured values for system recovery times; maximum values represent worst case system timing**
  - **1. Application startup**
    - Time from JM issues to JMA forks job
  - **2. Application failure**
    - Time from application failure to application recovery
  - **3. JMA failure**
    - Time from JMA failure to application recovery
  - **4. Node failure**
    - Time from Node, OS or High Availability Middleware failure to application recovery

Note: All times shown in seconds	Minimum	Average	Maximum	Std. Dev.
Reload/start application (1)	0.074	0.160	0.371	0.084
Application hang/crash/data error (2)	0.742	0.838	1.297	0.095
JMA hang/crash with application (3)	0.584	0.899	1.463	0.202
Node/OS/SR hang/crash (4)	51.201	52.148	53.191	0.744

TRL5 Demonstrations

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Demo	Mission	Processing Type	Timing	Fault Detect Mode	Recovery Mode	Fault Coverage	Criteria
1	LUD	Serial	none	none	Restart (CP N/A)	AJHC	3.2
2	LUD	Serial	none	3TR	Vote and RF	AHJC+DE	3.2
3	LUD	Serial	RTD	3SR	Vote and RB	AHJC+DE	3.2
4	LUD	Serial	none	ABFT	ED1	AHJC+DE	3.2
5	LUD	Serial	none	ABFT+3TR	ED1+Vote and RF	AHJC+DE	3.2
6	LUD	Serial	RTD	ABFT+3SR	ED1+Vote and RB	AHJC+DE	3.2
7	FTMM	Serial	RTD	ABFT	EC or Restart	AHJC+DE	3.2
8	2DFFT	Serial	none	none	Restart (CP N/A)	AJHC	3.2
9	2DFFT	Serial	none	3TR	Vote and RF	AHJC+DE	3.2
10	2DFFT	Serial	RTD	3SR	Vote and RB	AHJC+DE	3.2
11	LUD-P	Parallel	none	none	RB without CP	AHJC	3.1, 4.4
12	LUD-P	Parallel	none	3TR	Vote and RF	AHJC+DE	3.1, 4.4
13	LUD-P	Parallel	RTD	3SR	Vote and RB	AHJC+DE	3.1, 4.4
14	LUD-P	Parallel	none	ABFT	ED2	AHJC+DE	4.4
15	LUD-P	Parallel	none	ABFT+3TR	ED2+Vote and RF	AHJC+DE	4.4
16	LUD-P	Parallel	none	ABFT+3SR	ED2+Vote and RB	AHJC+DE	4.4
17	2DFFT-P	Parallel	none	Rebuild	RCP	AHJC+DE	3.1, 4.4
18	2DFFT-P	Parallel	none	3TR	Vote and RF	AHJC+DE	3.1, 4.4
19	2DFFT-P	Parallel	none	3SR	Vote and RB	AHJC+DE	3.1, 4.4
20	LUD,2DFFT,LUD,2DFFT	Sequentially Serial	RTD	ABFT,2SR,3SR,3TR	RF,RB,RB,RF	AHJC+DE	3.3
21	LUD,2DFFT+2DFFT,LUD	Sequentially Distributed	RTD	ABFT,2SR+2TR,2SR	RF,RB+RF,RB	AHJC+DE	3.3
22	2DFFT+LUD-P	Distributed Serial/Parallel	none	2SR+2TR	RCP + Vote and RF	AHJC+DE	3.4, 4.2
23	2DFFT-P+LUD	Distributed Serial/Parallel	none	2TR+2SR	RCP + Vote and RF	AHJC+DE	3.4, 4.2
24	LUD,LUD	Serial	RTD	Env. Adaptable SR	Vote and RB	AHJC+DE	N/A
25	Kmeans	Parallel	none	none	Abort	none	N/A
26	LUD+System Diagnostic	Serial	RTD	Frame Scheduling	RB+Abort	Mission	3.5
27	2DFFT (Chain of 4)	Serial	RTD	3SR,2TR,3SR,2TR	Vote and RB	AHJC+DE	4.7
28	2DFFT-FPGA	Serial	none	none	RB without CP	none	5
29	2DFFT-FPGA	Serial	none	HW TMR	Vote and RB	FPGA FT	6
30	2DFFT-FPGA	Serial	none	Threaded Replication	Vote and RB	FPGA FT	6
31	2DFFT-FPGA	Master/Slave Distributed	none	HW TMR	Vote and RF	FPGA FT	6
32	LUD-P	Parallel	none	3TR	Vote and RF	Network failover	4.7
33	LUD	Serial	none	Processor Signals	Abort	AHJC+DE+CE	3.2, 4.6

CP N/A = CP not avalilable in Serial 2DFFT and LUD
AJHC = Application and JMA Hang and Crash
FBS = Frame-based scheduling
RTD = Real-time Deadline

TR = Temporal Replication
SR = Spatial Replication
CP = Check Point
RCP = Restart from CP

RF = Roll Forward
EC = Error Correct
CE = Control Error

RB = Roll Back
ED1 = Error Detect and 1 Restart
DE = Data Error
ED2 = Error Detect and Abort

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DM Flight Experiment Objectives

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- **The objectives of the Dependable Multiprocessor experiment:**

  1) **to expose a COTS-based, high performance processing cluster to the real space radiation environment**

  2) **to correlate the radiation performance of the COTS components with the environment**

  3) **to assess the radiation performance of the COTS components and the Dependable Multiprocessor system response in order to validate the predictive Reliability, Availability, and Performance models for the Dependable Multiprocessor experiment and for future NASA missions**

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ST8 Spacecraft – "NMP Carrier"

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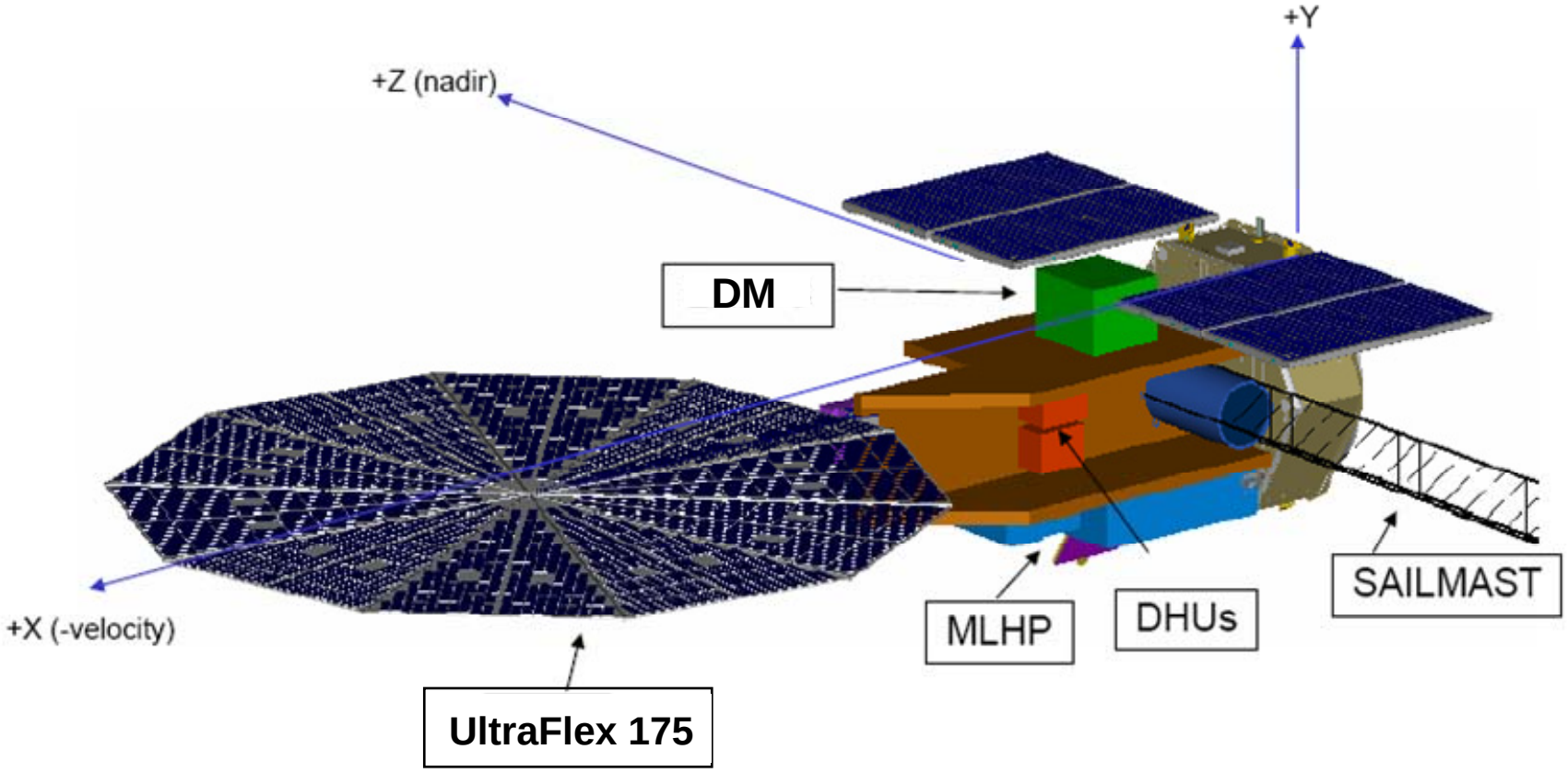

ST8 Orbit: - sun-synchronous
- 320km x 1300km @ 98.5° inclination
- selected to maximize DM data collection

Note: Sailmast is being moved to +X direction to minimize drag after deployment; Sun is (nominally) in the +Y direction

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DM Flight Experiment Unit

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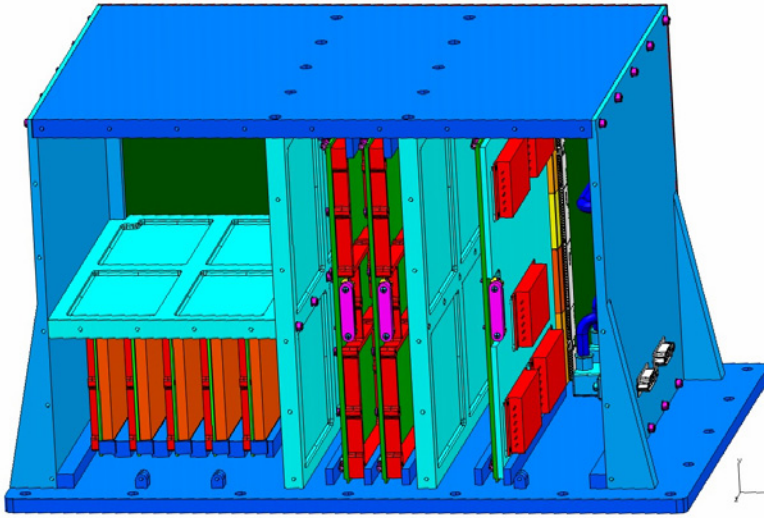
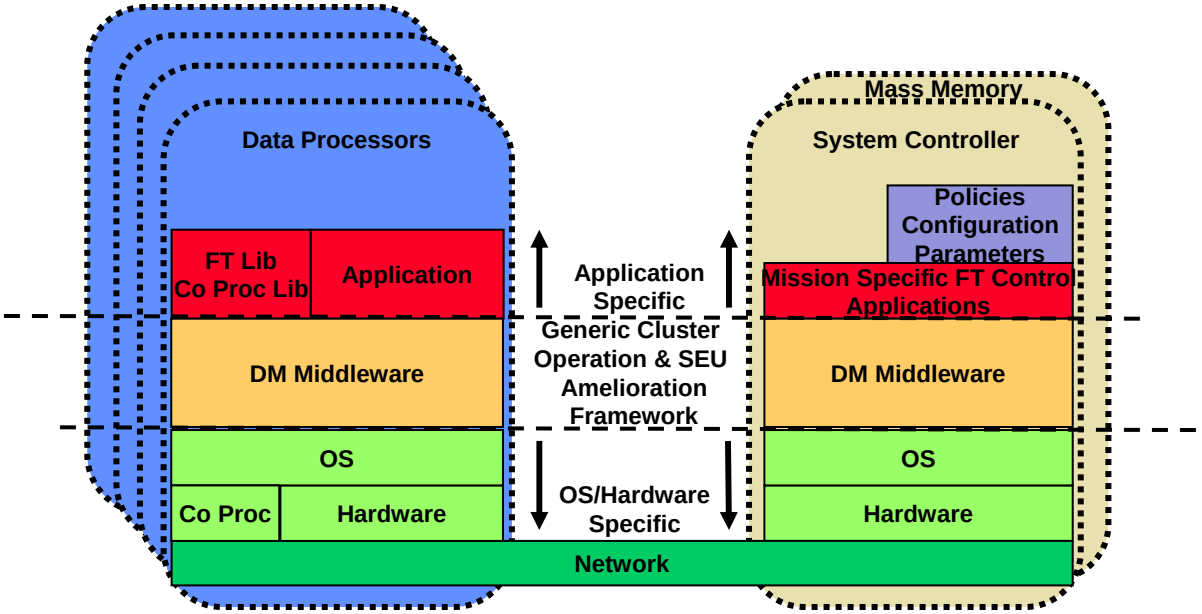


- 1 RHPPC SBC System Controller node
- 4 COTS DP nodes
- 1 Mass Storage node
- Gigabit Ethernet interconnect
- cPCI
- ST8 S/C interface
- Utility board
- Power Supply

Hardware

- Dimensions
  - 10.6 x 12.2 x 18.0 in. (26.9 x 30.9 x 45.7 cm)
- Weight (Mass)
  - ~ 42 lbs (19 kg)
- Power
  - ~ 100 W



Software

- Multi-layered System SW
  - OS, DM Middleware, APIs, FT algorithms
- SEU Immunity
  - detection
  - autonomous, transparent recovery
- Multi-processing
  - parallelism, redundancy
  - combinable modes

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Ultimate Fully-Scaled DM – 'Superset' of Flight Experiment

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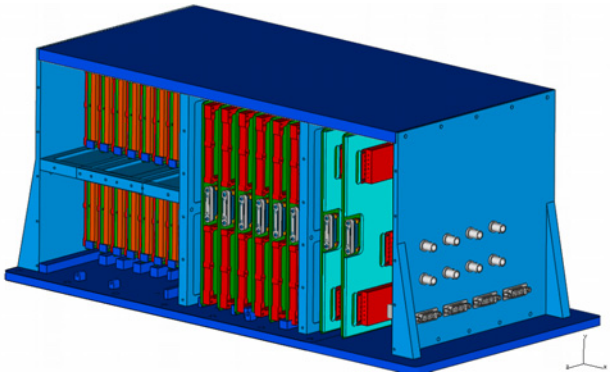
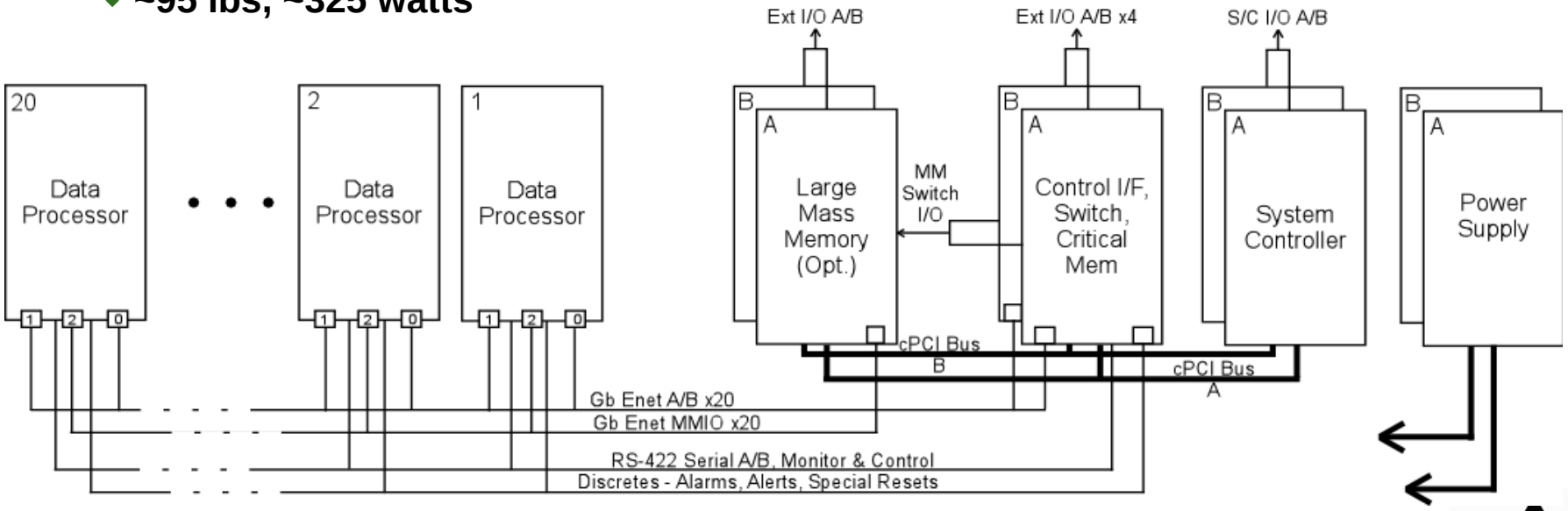
- **Architecture Flexibility:**
  - Any size system up to 20 Data Processors
  - Internally redundant common elements (Power Supply, System Controller, etc.) are optional
  - Mass Memory is optional; DM is flexible; can work with direct IO and/or distributed memory (w/redundantly stored critical data), as well
- **Scalable to > 100 GOPS Throughput**
  - All programmable throughput
  - ~95 lbs, ~325 watts





Summary & Conclusion

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- **Flying high performance COTS in space is a long-held desire/goal**
  - Space Touchstone - (DARPA/NRL)
  - Remote Exploration and Experimentation (REE) - (NASA/JPL)
  - Improved Space Architecture Concept (ISAC) - (USAF)
- **NMP ST8 DM project is bringing this desire/goal closer to reality**
- **DM project successfully passed key NMP ST8 Phase B project gates**
  - TRL5 Technology Validation Demonstration
  - Experiment-Preliminary Design Review (E-PDR)
  - Non Advocate Review (NAR)
- **DM qualified for elevation to flight experiment status; ready to move on to Phase C/D (flight)**
- **DM technology is applicable to wide range of missions**
  - science and autonomy missions
  - landers/rovers
  - UAVs/USVs/Stratolites/ground-based systems
  - ORS (Operationally Responsive Space)
  - rad hard space applications
- **Unlike previous attempts to migrate high performance COTS processing to space (Space Touchstone, REE, ISAC), the NMP ST-8 program has "legs"**
  - NASA NMP is providing the ride
  - Orbital Science Corporation has been selected to be the S/C provider
  - Pegasus has been selected as the launch vehicle

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