Leveraging Carbon Nanotubes to Develop a Fourth-Generation Radiation Hardened Microprocessor for Space

Richard Ridgley
rridgley@adelphia.net

The High Performance Embedded Computing Workshop

September 2006

Outline

- Current Space Processors and Issues
- Key Carbon Nanotube Features
- Carbon Nanotubes for Memory and Logic
- Performance Expectations
- Microprocessor Roadmap
- Other Leveraging Opportunities
- Conclusions

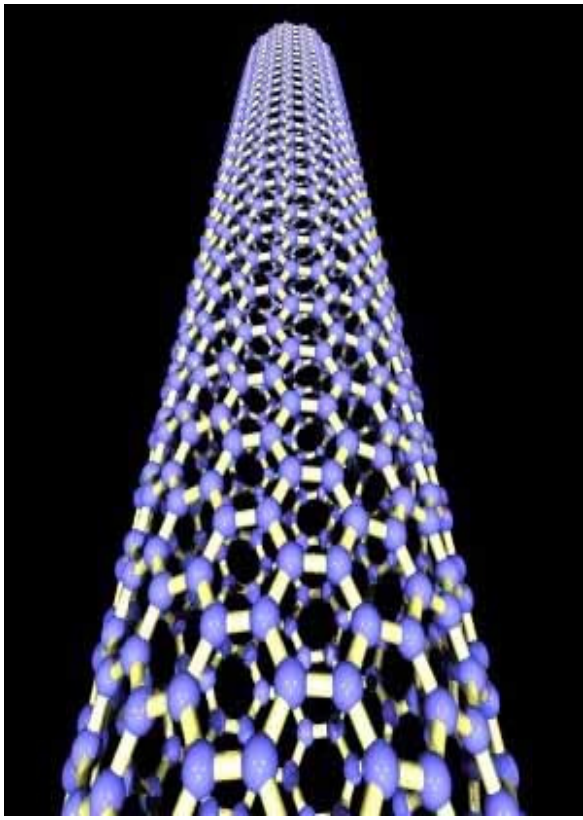
Current Processors and Issues

- **Space mission complexity is increasing**
- **Current radiation hardened processor:**
  - 400 MIPS Future Generation-High Performance Spaceborne Computer (FG-HPSC) developed at BAE Systems
- **Need exists for advanced performance microprocessor that must survive severe radiation threats**
  - Electrical performance desired: 1BIPS at 5 Watts
  - Radiation performance desired:

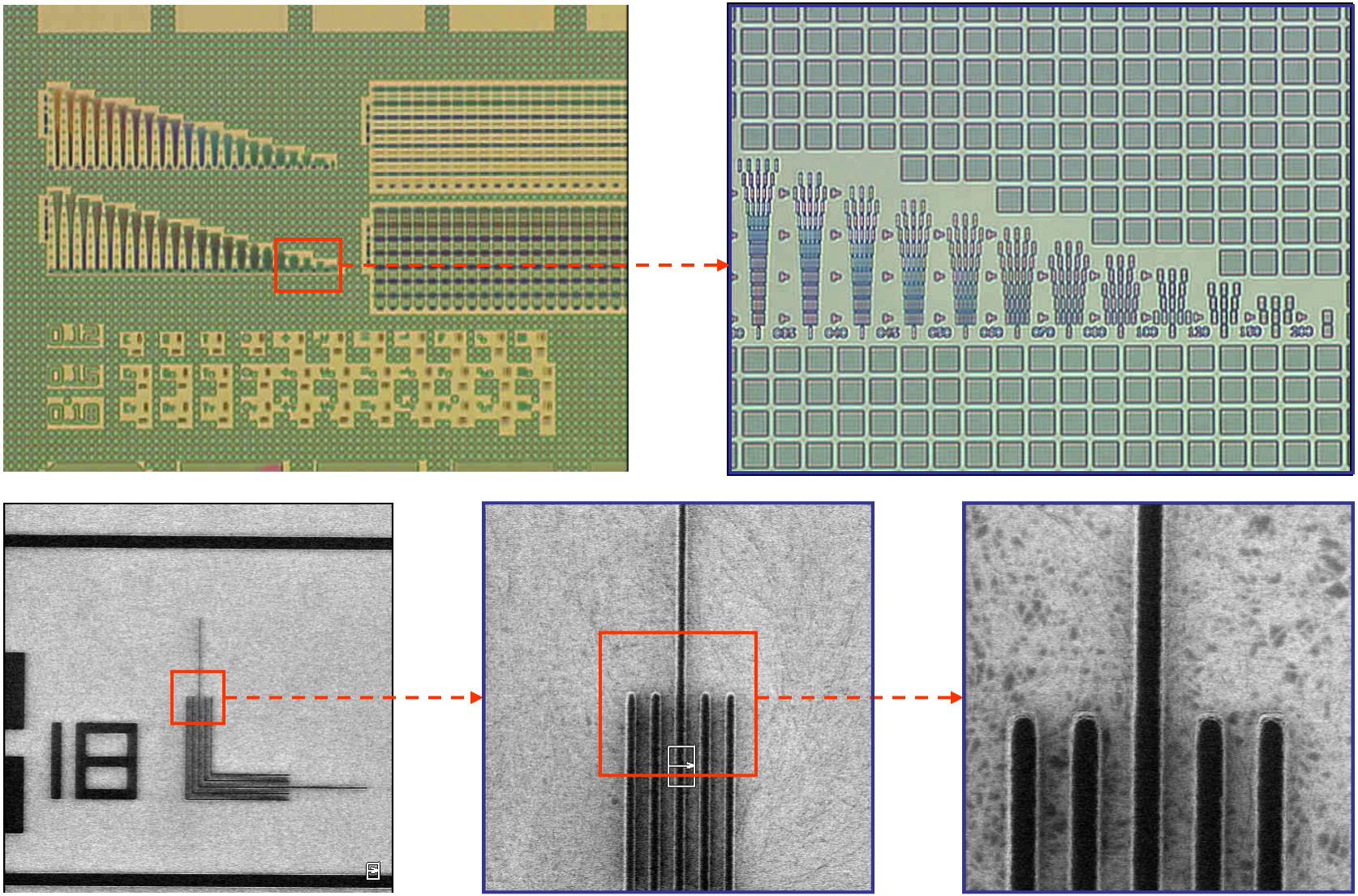
Parameter	Level
Total Dose	**>1 Mrad(Si)**
Single Event Upset	**$<10^{-11}$ errors/bit-day**
Single Event Latchup	**>120 MeV-cm^2/mg**
Neutron	**$>10^{13}$ n/cm^2**
Dose Rate Upset	**$5x10^9$ rad(Si)/sec**
Dose Rate Survive	**10^{12} rad(Si)/sec**

Key Carbon Nanotube Features

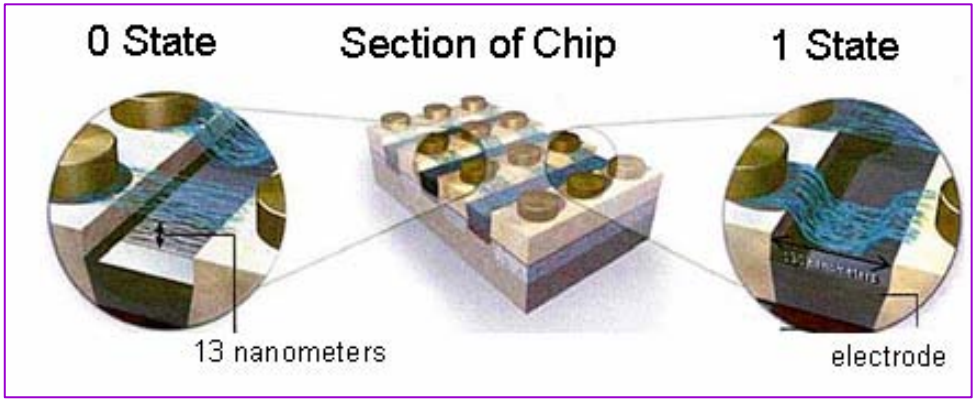
- **Basic properties**
  - **CNT: ~ 1 nm diameter metal / semiconductor**
  - **Current density: 10^9 A/cm^2**
  - **Thermal conductivity: ~diamond**
  - **Mechanical strength: 100x stronger than steel**
- **Carbon nanotube growth is tailored**
  - **Nanotube fabric sheet density and resistance depend on fabrication methodology**
- **Inherently radiation hard**
- **Electrical properties and material strength enable use as nano-electromechanical switch**
- **Material and lithographic compatibility with CMOS process**
  - **Room temperature deposition by spin coating**
  - **Robust metallization (sputter/CVD)**



Lithographic Patterning of Carbon Nanotube Fabrics

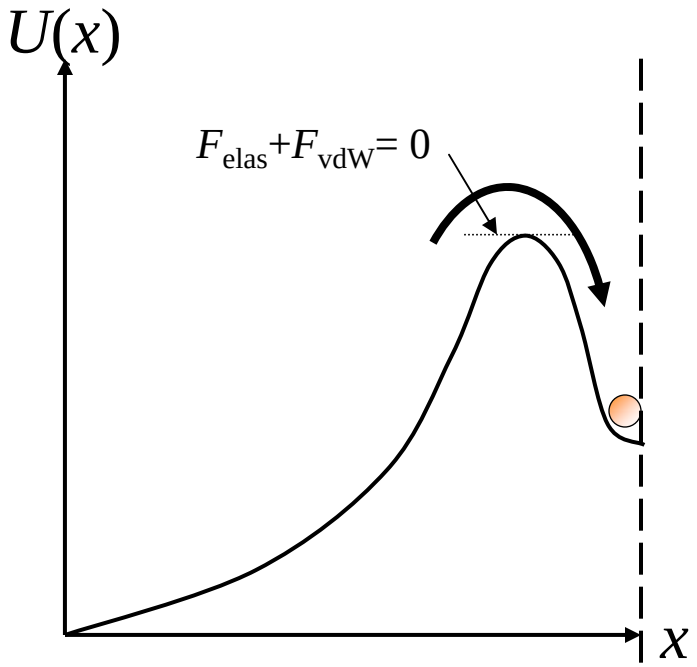


Carbon Nanotubes for Memory and Logic

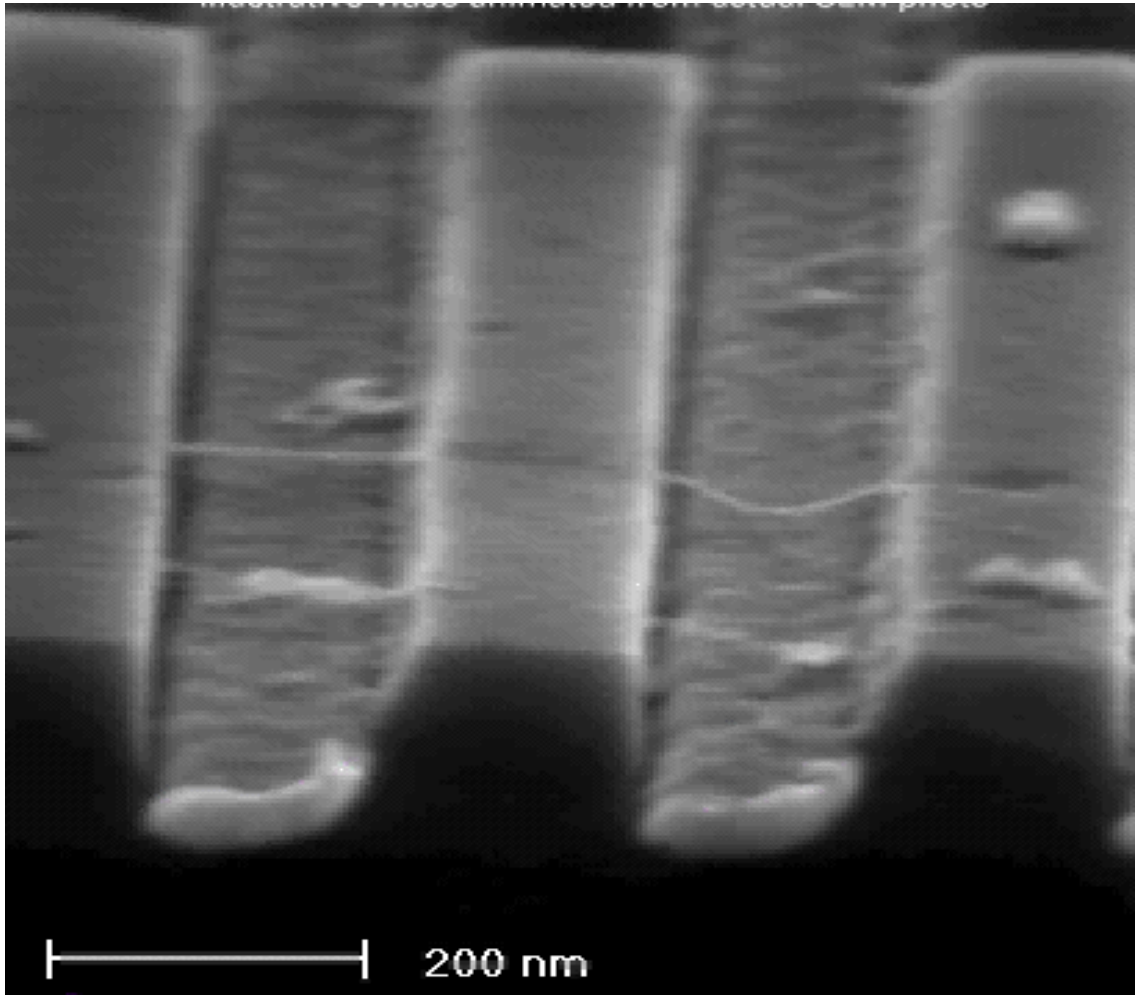


- **Operation**
  - **Switching occurs by applying an electric field between the write/read electrode and the CNT fabric**
  - **Field deforms the CNT fabric until contact is made with the write/read electrode.**
  - **Contact defines an ‘on’ device and the junction resistance can be read**
  - **CNT fabric remains in place by van der Waals forces**
- **Key Results**
  - **Switched bits are nonvolatile--volatile designs also exist**
  - **No standby current; no leakage current**
  - **One switch replaces 6-12 transistors for memory**

Illustration of 3-Term Electromechanical switch Operation Using Molecular van der Waal's Forces

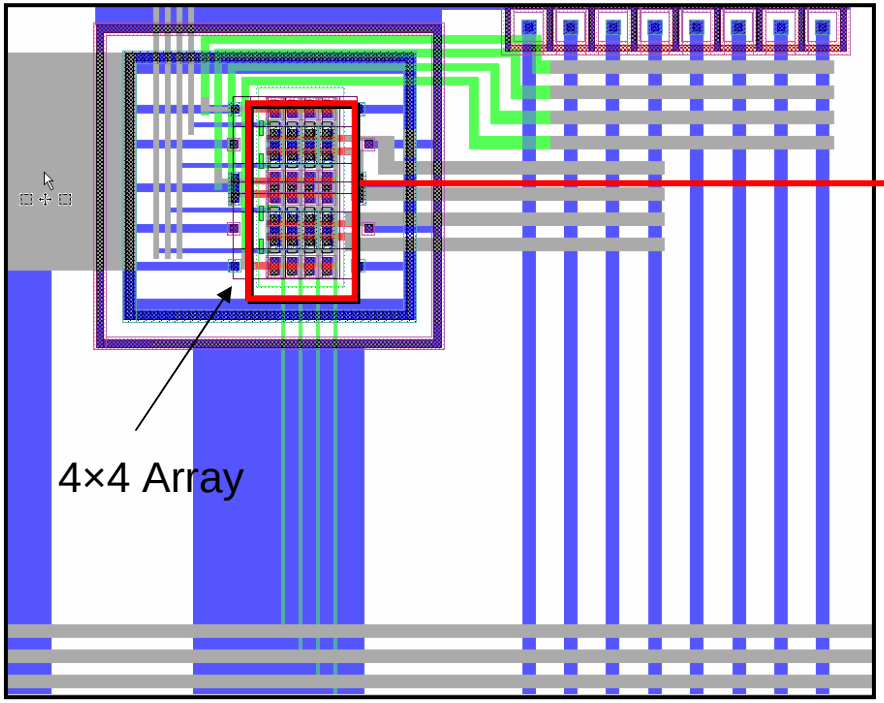


Nanotube memories *<u>are</u>* **nonvolatile** *devices*

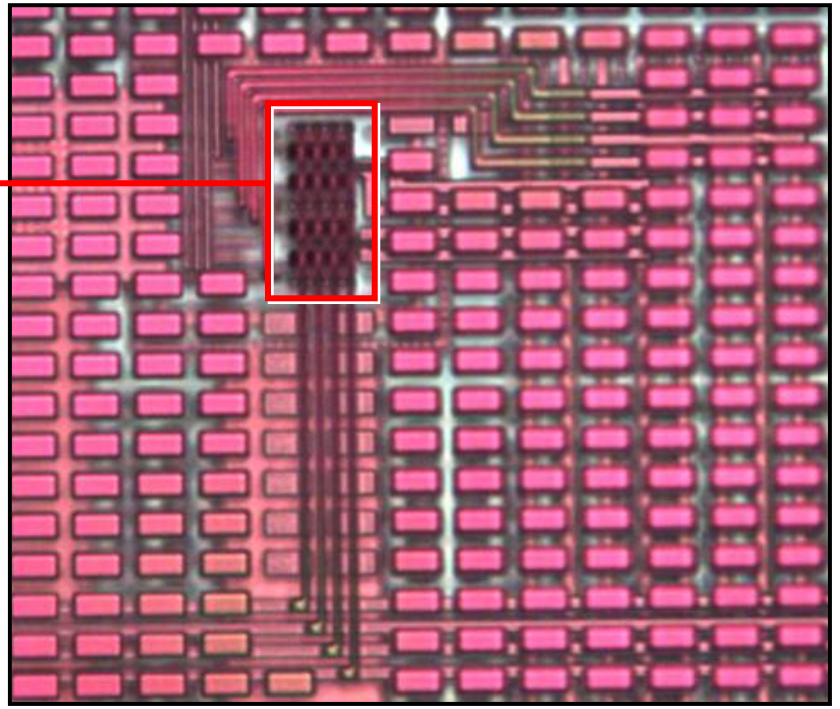


16-bit Nonvolatile Memory CMOS Array (4×4)

Mask Layout

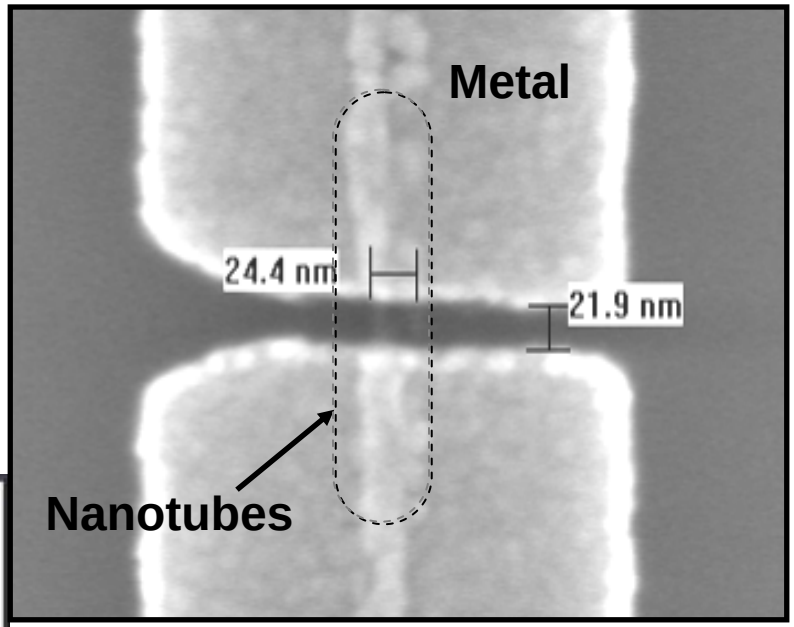


Die Photo

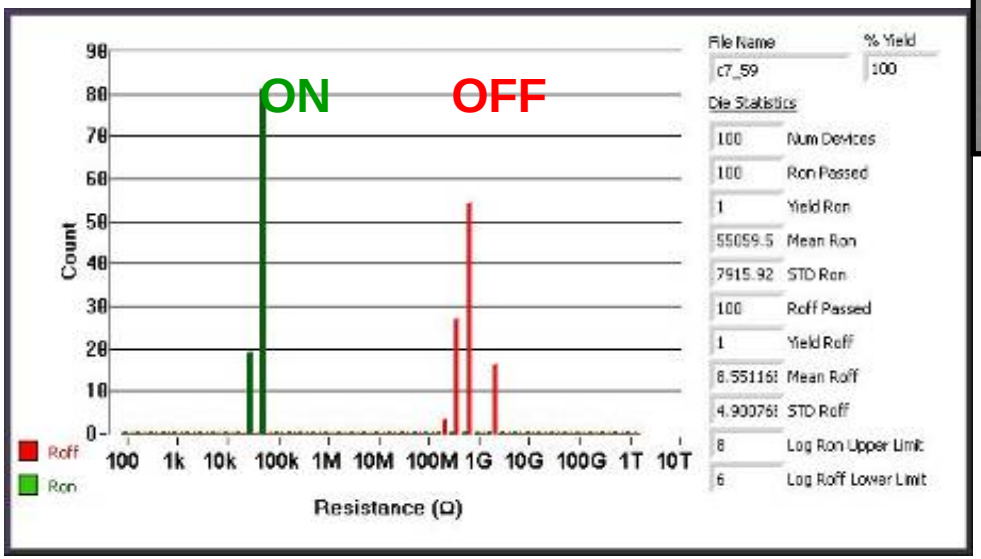


Nonvolatile Memory Operation – Device Scaled to 20 nm

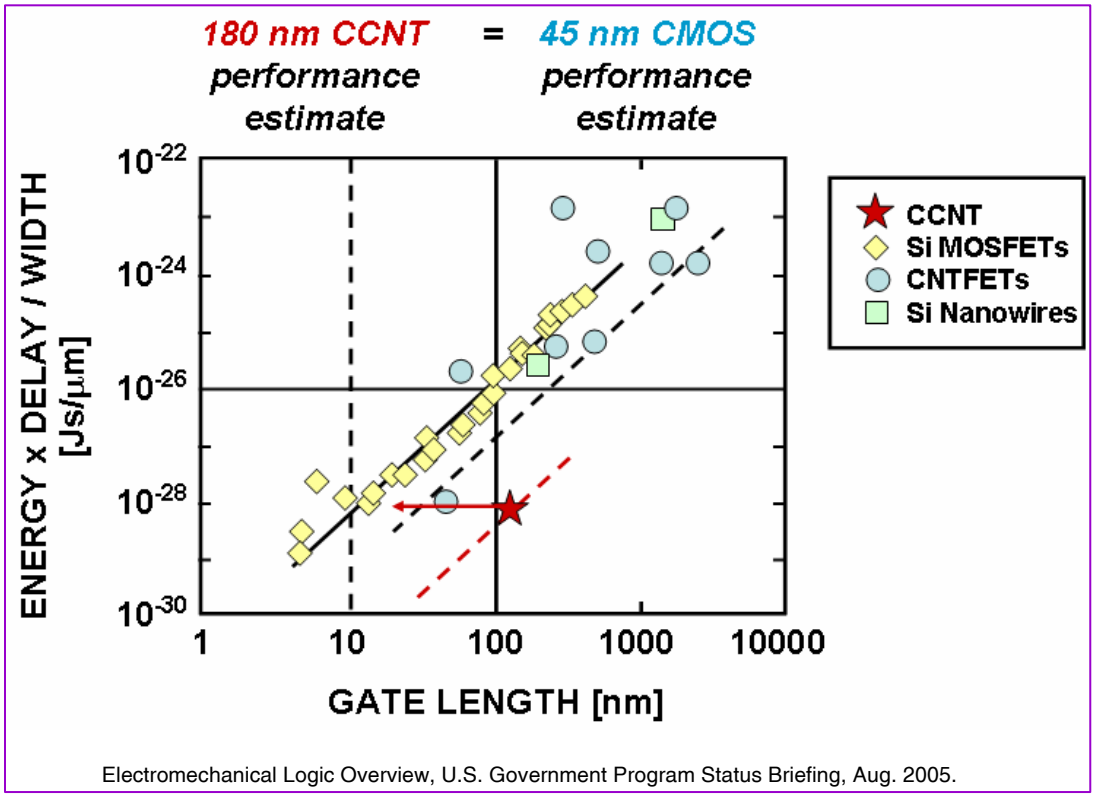
- **Nanotube fabric length: 22 nm**



Top down view



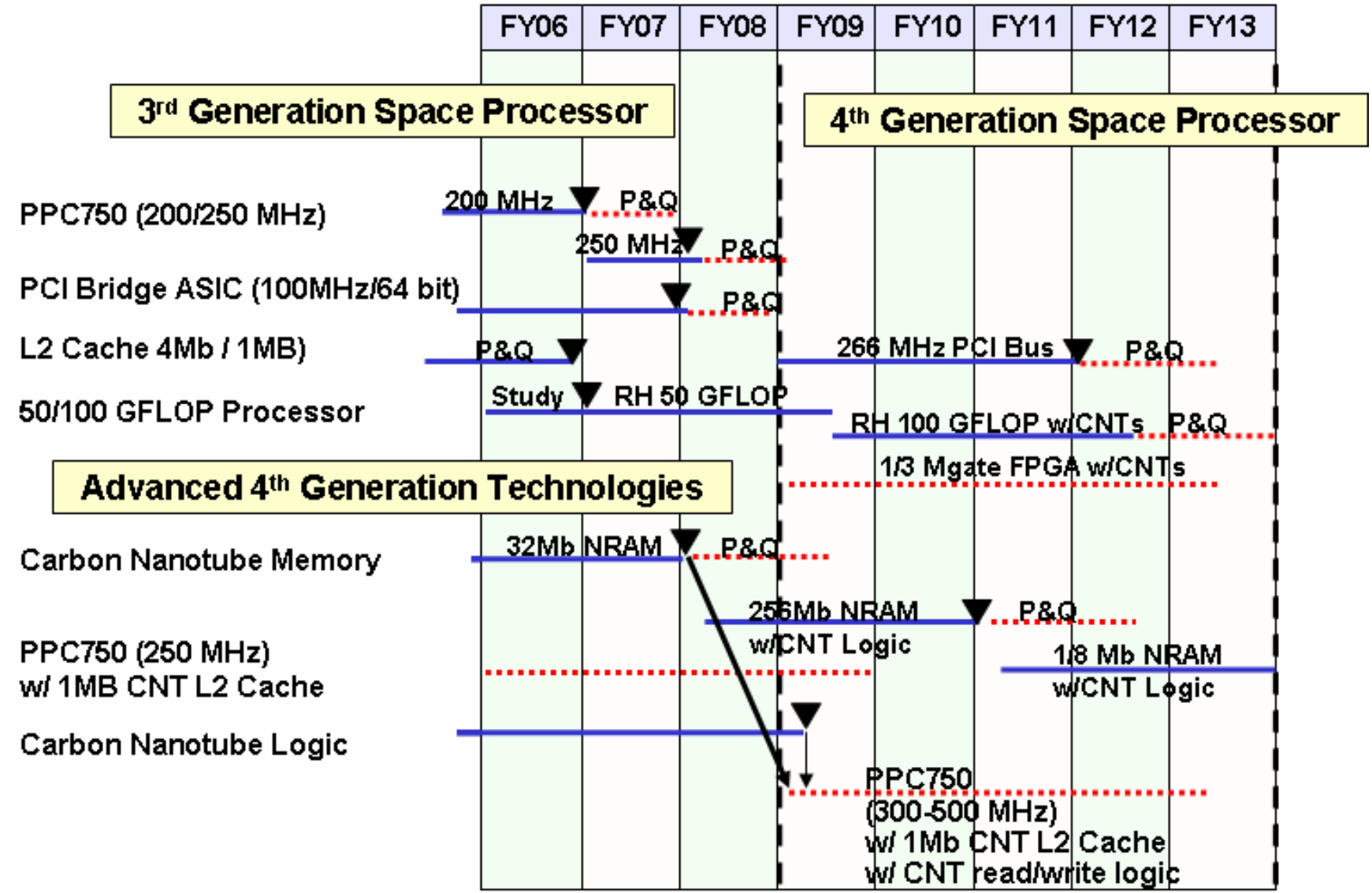
Performance Expectations



Electromechanical Logic Overview, U.S. Government Program Status Briefing, Aug. 2005.

- **For a given lithography node, CNT devices can enable:**
  - **80% reduction in cell area and more if multi-layers are used**
  - **10x increase in gate speed, and**
  - **5x decrease in overall power at speed**

Radiation Hardened Microprocessor Roadmap



Other Leveraging Opportunities

Potential CNT integration and redesign projects include:

- **Non-volatile 3M-gate FPGAs**
- **Large non-volatile memory chips, 256Mb/1Gb/8Gb**
  - **For very large solid state recorders (SSR) and memory buffers**
- **Dual core Power PC 750 250 MHz with dual on-chip 1-MB L2 cache**
  - **Also replace**
    - **Buffers,**
    - **Registers,**
    - **L1 cache (32KB data and instruction) and**
    - **Read/write logic (memory management units)**
  - **Achieve 1 billion instructions per second at 5 watts of power**
- **Vector processor (e.g. CSX600) by replacing SRAM memory and read/write logic to allow 128 each, 32 bit floating point processing units. This will allow**
  - **100 billion floating point calculations per second in space**
- **Replace ASIC memories and read/write logic for enhanced performance, reduced power and part cost**

Conclusions

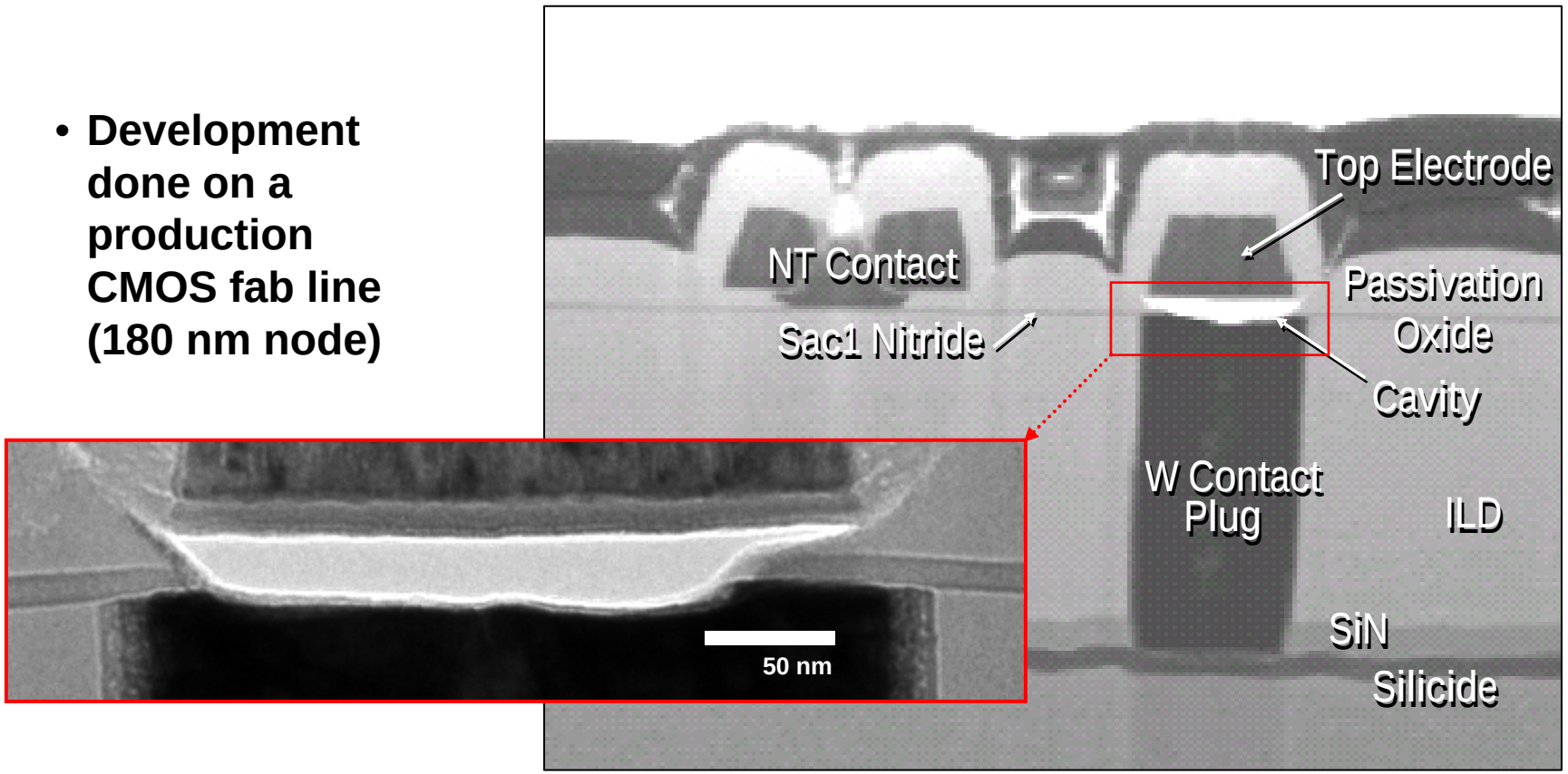
- **CNT technology offers a unique opportunity to rapidly advance radiation hardened memory and logic capabilities**
- **Enables low power advanced electronics for use in space**
- **CMOS compatibility enables advanced performance at established radiation hardened foundries without additional capital investment**
- **Offers a path forward to quickly address the rapidly advancing space processing needs**

Backup Slides

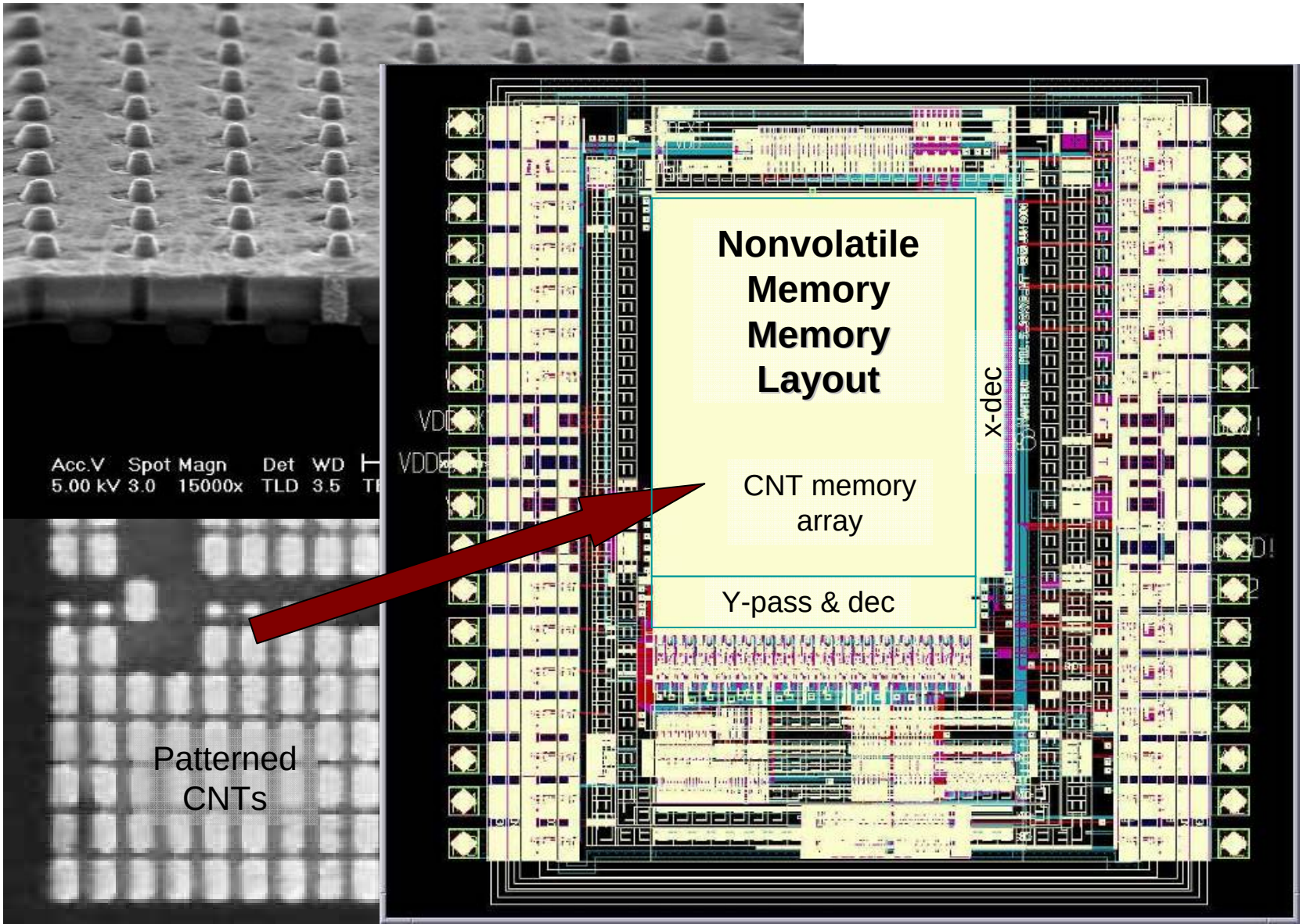
3-Term Nonvolatile Memory Technology

- **Self-passivated nanocavity for nonvolatile memory devices allows standard packaging**

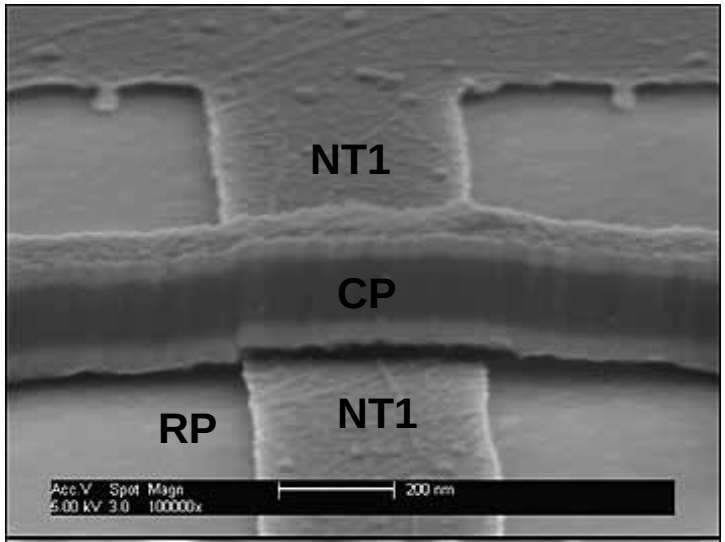
- **Development done on a production CMOS fab line (180 nm node)**

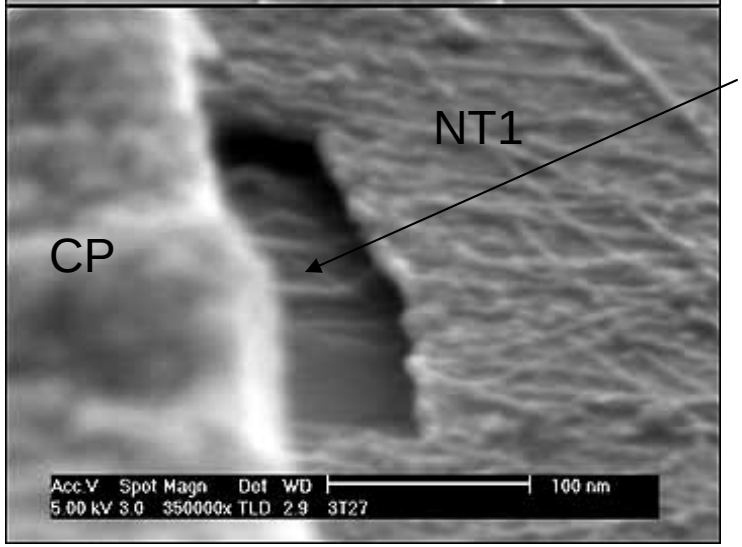


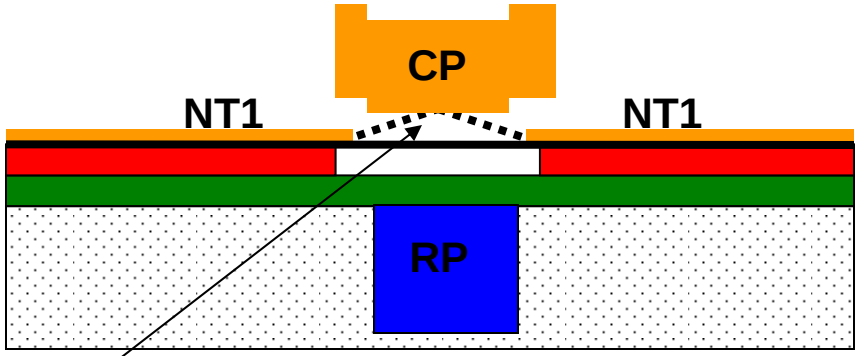
Snap Shot of Layout



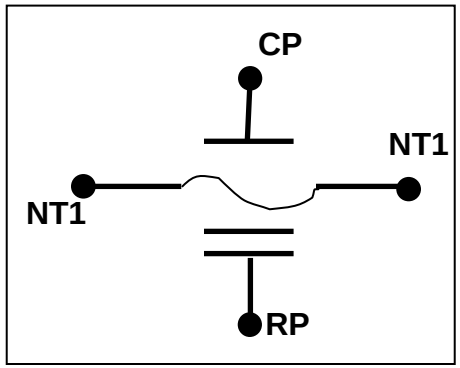
R&D Nonvolatile Memory Devices







Suspended CNTs



Nonvolatile Memory Characteristics

Property	Performance
Intrinsic Bit Speed	2 -3 GHz
Permanent Non-volatility	Yes
Read Access Time	<5 ns
Write/Erase Access Time	<5 ns
Standby Current (ma)	0
Power Consumption	~0.2 mW
Max # Read/Write Cycles	infinite
Retention	>10 years
Ease of CMOS Integration	high
Operating Temperature	-273C to +250C
Resistant to Magnetism	Yes
Resistant to Vibration	Yes
Multi-bit storage	Yes
Maximum Potential Speed	200 GHz
Maximum Theoretical Destiny/Area (b/cm^2)	1000G
Process Complexity	Low