Leveraging Carbon Nanotubes to Develop a Fourth-Generation Radiation Hardened Microprocessor for Space

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Introduction

Space mission complexity is increasing and results in significant developmental challenges for advanced performance microelectronics that must survive radiation threats while operating in a constrained trade space involving size, weight, power, and heat dissipation. The use of a disruptive technology, carbon nanotubes (CNT), in embedded memory and logic circuits enables unique opportunities to enhance both the electrical and radiation performance of legacy and current state-of-the-art foundry processes.[i] This paper will discuss the research development path planned for the use of carbon nanotubes to enable a one-billion instruction-per-second general purpose microprocessor capable of surviving the highest radiation levels anticipated by the U.S. Government.

Current State of Practice

The U.S. Government employs a centralized research and development roadmap to coordinate radiation hardened microelectronics development and qualification for space use. The current leading edge radiation hardened microprocessor is the 400 million-instructions-per-second Future Generation-High Performance Spaceborne Computer (FG-HPSC) developed at BAE Systems in Manassas, VA. The FG-HPSC is commonly referred to as the RAD 750 because of its heritage from the PPC750. The RAD750 is the core of the U.S. Government's third-generation space 5-Watt processor development effort which includes developments for the PCI bridge ASIC (100MHz/64 bit) and integration of a 4Mb L2 cache. This development has occurred on a radiation hardened process that meets the radiation specifications shown in Table 1.

Table 1: Relevant Legacy Radiation and Performance Metrics.

Parameter	Level
Technology Node	150nm Bulk CMOS
Operating Temperature	Full Performance: 0 to 80C Functionality: -55 to 125C
Operating Speed	Post radiation: 1GHz
Operating Voltage	1.5, 1.8, 2.5V
Total Dose	>1 Mrad(Si)
Single Event Upset	$<10^{-11}$ errors/bit-day
Single Event Latchup	>120 MeV-cm^2/mg
Neutron	$>10^{13}$ n/cm^2
Dose Rate Upset	$2x10^9$ rad(Si)/sec
Dose Rate Survive	10^{12} rad(Si)/sec

Advancing radiation hardened electronics performance to that of commercial electronics for 90nm and below requires costly investments in a) capital equipment, b) hardening-by-design techniques and infrastructure, or c) an innovative means to increase the performance of existing foundries through the integration of novel materials, process, design, and layout changes.

Carbon Nanotube Electromechanical Switches

Complementary Carbon Nanotube Logic (CCNL) addresses the major roadblocks to the future space use of CMOS logic: CCNL is inherently radiation hard and does not draw standby power. CCNL is an extension technology that will replace memory (SRAM, DRAM, Flash), buffers, registers, and read/write logic circuits normally built in CMOS. CCNL is completely compatible with silicon CMOS manufacturing and requires no additional capital investment. The basic electromechanical nature of CNT device is shown in Figure 1.

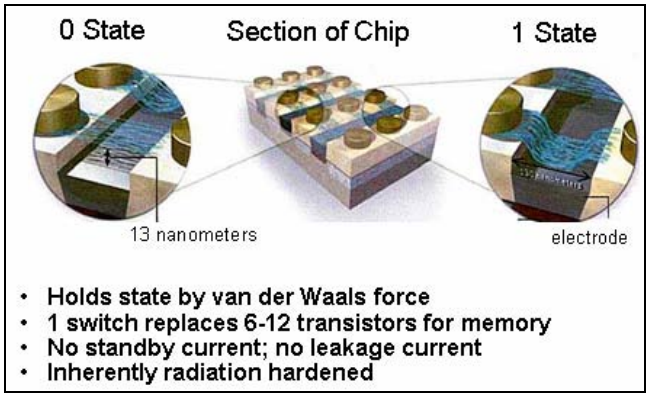

Figure 1: CNT as an Electromechanical Switch. [ii]

Switching occurs by applying an electric field between the write/read electrode and the CNT fabric. This field deforms the CNT fabric until contact is made with the write/read electrode. This contact defines an 'on' device and the junction resistance can be read.[iii] At this point the electric field is turned off and the CNT fabric remains in place by van der Waals forces; the switched bits are nonvolatile. Volatile designs also exist. Changing state requires application of an electric field to a release electrode not shown in the diagram. Designs have been developed for electromechanical pull-up/pull-down and transfer device for logic applications. Total dose testing of CNT memory devices with ^{60}Co γ-rays showed the ability to retain data for doses as much as 10 Mrad(Si).[iv]

The desire to achieve advanced commercial electronics performance on a 150nm radiation hardened foundry

process becomes possible when one realizes that, for a given lithography node, CNT devices will enable:

- up to 80% reduction in cell area and more if multi-layers are used
- up to 10x increase in gate speed, and
- up to 5x decrease in overall power at speed.

Figure 2 shows performance metrics predicting that an 180nm CNT lithography node can yield performance that is equal to that of a commercial 45nm CMOS process.

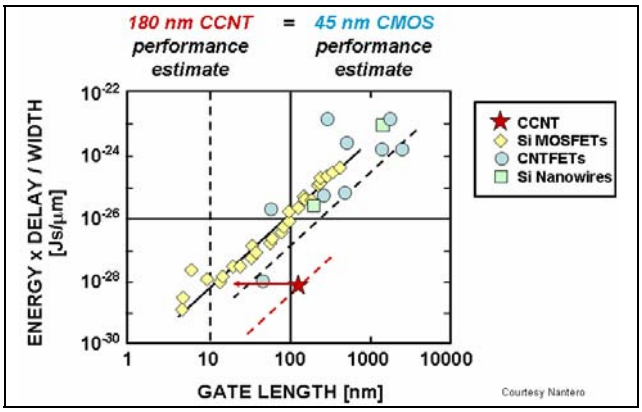

Figure 2: Performance: 180nm CCNL = 45nm CMOS. [v]

Roadmap to Leverage CNT Capabilities

The U.S. Government will take advantage of CNT's compatibility with CMOS processes to develop and transition a 4th generation general purpose space processor capable of one-billion instructions-per-second that can survive the highest radiation levels anticipated by the U.S. Government.

Potential integration and redesign projects include:

- Non-volatile 1- and 3-million gate Field Programmable Gate Arrays (FPGAs). Urgently needed by many space programs.
- Large non-volatile memory chips, 256 MegaBit (Mb), 1 GigaBit (Gb) and eventually 8 Gb. Required for very large future solid state recorders (SSR) and memory buffers.
- Dual core Power PC 750 250 MHz with dual on-chip 1 MegaByte L2 cache. Also replaces buffers, registers, L1 cache (32KB data and instruction) and read/write logic (memory management units). Will achieve 1 billion instructions per second at 5 watts of power.
- Vector processor (e.g. CSX600) by replacing SRAM memory and read/write logic to allow 128 each, 32 bit floating point processing units. This will allow 100 billion floating point calculations per second. This ability does not currently exist for space.
- Application specific integrated circuits (ASICs) will have their memories and read/write logic replaced for enhanced performance, reduced power and reduced part cost.

The order of the redesign efforts leveraging CNT technology will be determined by high priority space system needs. The microprocessor advancement program will build upon the successes of the current RAD750 program at BAE and integrate advances from the U.S. Government's 32Mb NRAM program. The new effort will provide space systems a dual core PPC750 with CNT read/write logic. The dual-core PPC750 will also be capable of addressing 1MB of integrated CNT L2 cache. Additionally, a research effort will examine the feasibility of replacing the aluminum wiring with CNT interconnects that are appropriately tuned to address resistance and capacitance issues.[vi] Figure 3 shows the projects and respective timing to provide these capabilities.

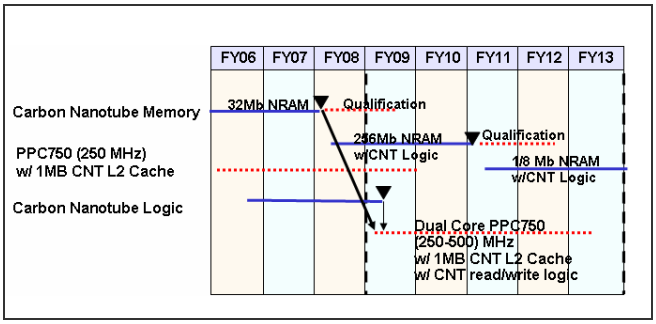

Figure 3: Roadmap Showing Planned CNT Developments.

Conclusion

Carbon nanotube technology offers a unique opportunity to allow the U.S. Government to "leapfrog" radiation hardened memory and logic capabilities to enable low power advanced electronics for use in space. The potential to use carbon nanotubes in conjunction with the established radiation hardened front-end-of-the-lines without the need for additional capital investment offers a path forward to quickly address the rapidly advancing space processing needs.

References

[i] J. Ward, et al., "A Non-Volatile Nanoelectromechanical Memory Element Utilizing a Fabric of Carbon Nanotubes," Proceeding 2004 Non-Volatile Memory Technology Symposium, pg 34-38, 17 Nov. 2004.

[ii] G. Stix, "Nanotubes in the Clean Room," Scientific American, Vol. 289, pg 82-85, Feb. 2005.

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[iv] M. N. Lovellette, et al., "Nanotube Memories for Space Applications," 2004 IEEE Aerospace Conference Proceedings, 2004.

[v] D. Brock, Nantero Electromechanical Logic Overview, U.S. Government Program Status Briefing, Aug. 2005.

[vi] M. Liebau, et al., "Electrical Interconnects Made of Carbon nanotubes," Synthetic Nanostructures, American Institute of Physics, pg 536-539, downloaded http:// proceedings.aip.org/ proceedings/cpct.jsp, Nov 2004.