# HPEC: Looking Back and Projecting Forward

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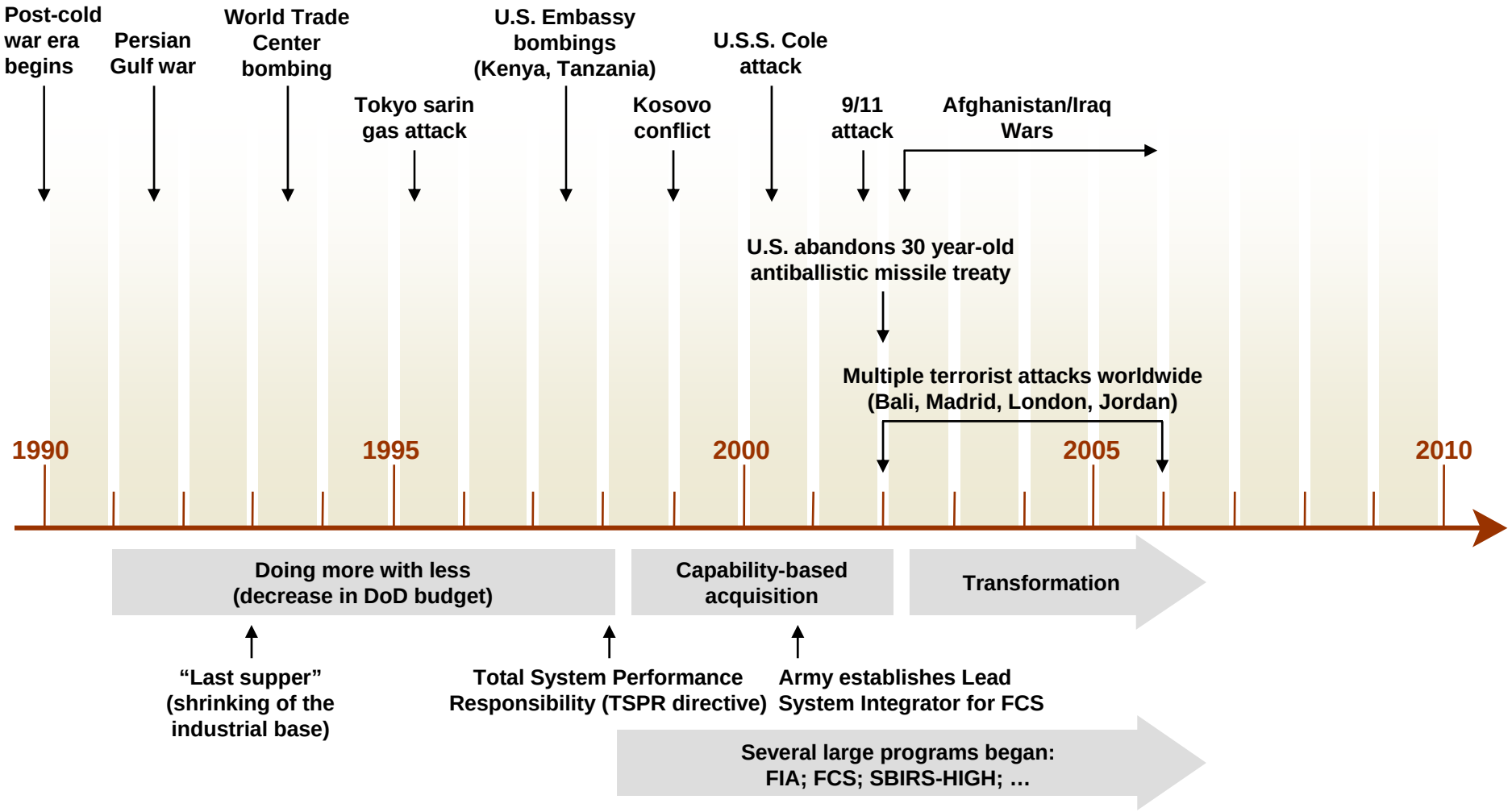
## 2006 High Performance Embedded Computing Workshop

**This work was sponsored under Air Force Contract FA8721-05-C-0002. Opinions, interpretations, conclusions and recommendations are those of the authors and are not necessarily endorsed by the Department of Defense.**

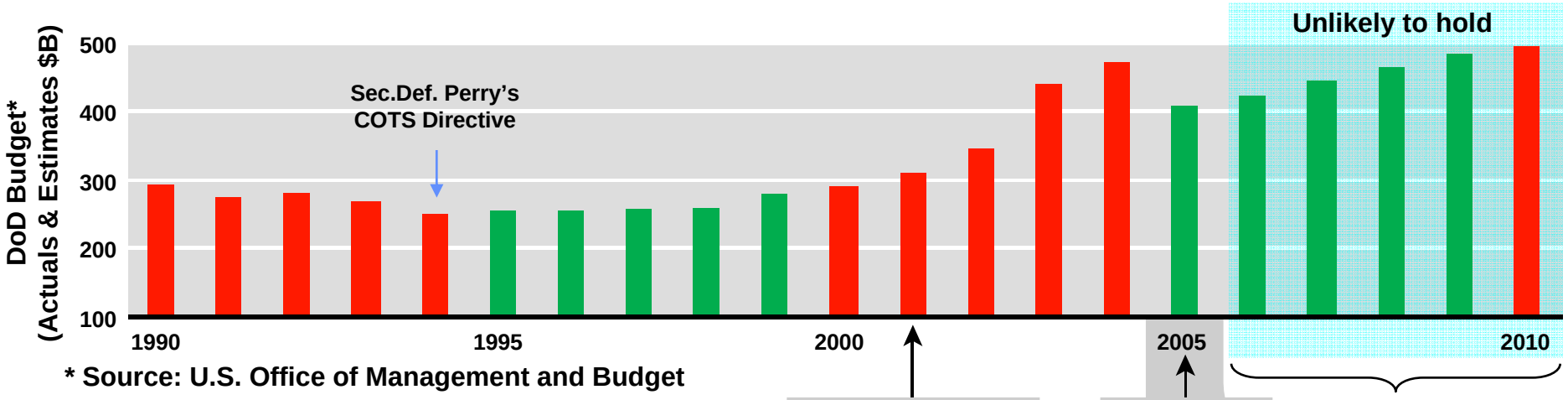
# Outline

- Big Picture Over Past Decade
- HPEC Representative Developments
- DoD Landscape and Impact on HPEC
- The Next Decade and Net-Centric Architectures
- Summary

# World Events and Directives Impacting DoD Investments



# DoD Budget and QDR Focus

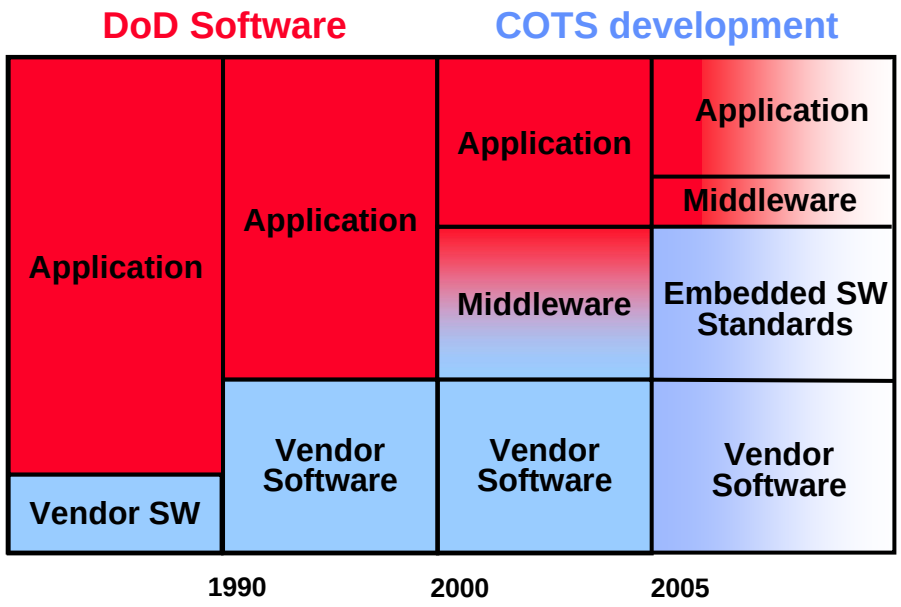


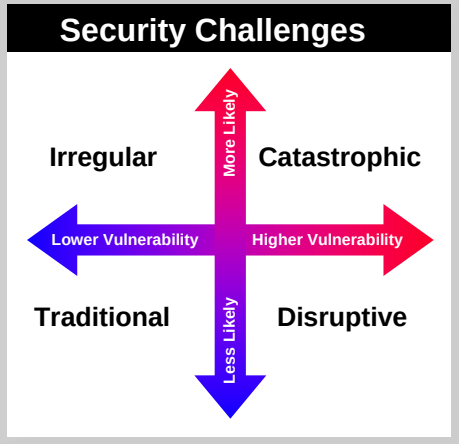

* Source: U.S. Office of Management and Budget

2001 Quadrennial Defense Review (from threat-based to capability-based acquisition)

2005 Quadrennial Defense Review

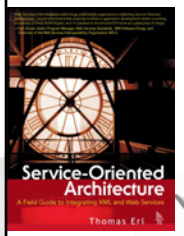
Reductions in next five years likely



# High Performance Embedded Computing

## - A Historical Perspective -

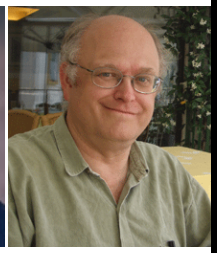
| 1997-1998 | 1999-2000 | 2001-2002 | 2003-2004 | 2005-2006 | 2007+ |
|---|---|---|---|---|---|
| **Computing Systems** | | | | | |
|  |   |   |   |   |    |
| **Intel Paragon & STAP Processor** | **AFRL HPCS & Improved Space Processor Architecture** | **NEC Earth Simulator & Mk 48 CBASS BSAR** | **LLGrid System & KASSPER** | **IBM Blue Gene & WorldScape Scalable Processing Platform** | **Net-centric / service-oriented architectures & unmanned platforms** |
| • 40-50 MHz clock<br>• <0.1 to 12 MFLOPS per watt | • 200-333 MHz clock<br>• 30-40 MOPS per watt | • 80-500 MHz clock<br>• 60-90 MFLOPS per watt | • 500 MHz - 2.8 GHz clock<br>• 65-320 MFLOPS per watt | • 250-700 MHz clock<br>• 200 MFLOPS – 100s GFLOPS per watt | • 1000s GFLOPS per watt |
| **Enabling Technologies** | | | | | |
| • VSIPL & MPI standards<br>• Adaptive Computing Systems / Reconfigurable Computing | • Data Reorg forum<br>• High-performance CORBA<br>• VLSI Photonics<br>• Polymorphous Computing Architectures | • High-performance embedded interconnects<br>• Parallel MATLAB<br>• Cognitive Processing<br>• Integrated ASICs, FGPAs, and prog. devices | • Grid computing<br>• VXS (VME Switched Serial) draft standard | • VSIPL++ standard<br>• Multi-core processors | • Self-organizing wireless sensor networks<br>• Global Information Grid<br>• Distributed computing and storage |

# HPEC Workshop Highlights

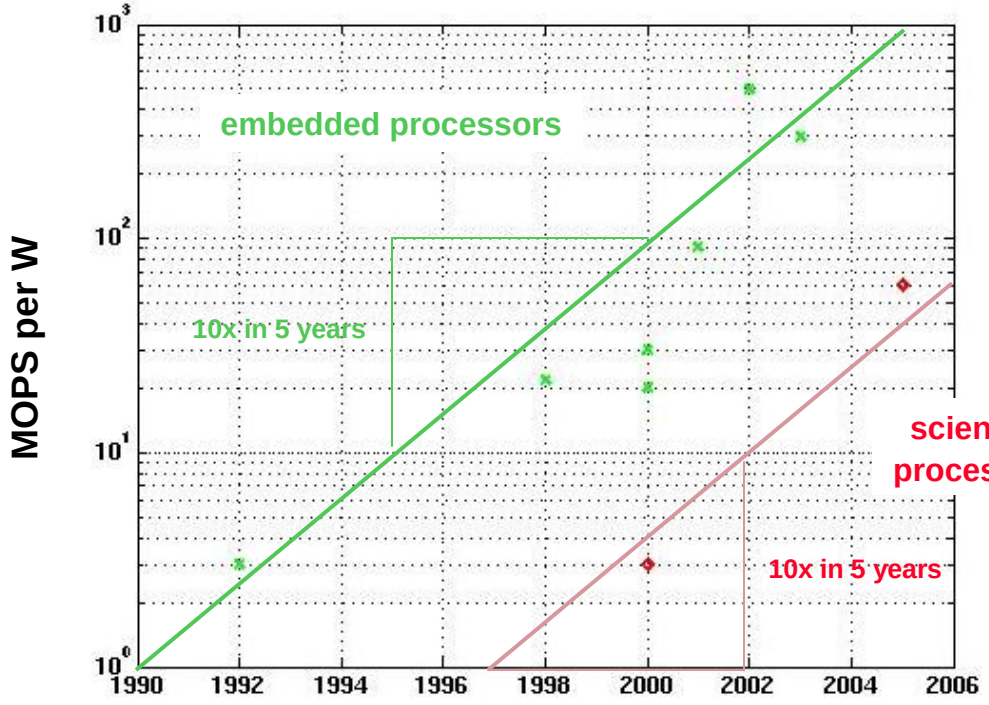
**1997**
- keynote: RADM K. Paige, USN
- 1st HPEC
- VSIPL API v1.0 released

**1998**
- keynote: F. Perry, SPAWAR
- 1st session dedicated to reconfigurable computing
- MPI/RT API v1.0 released

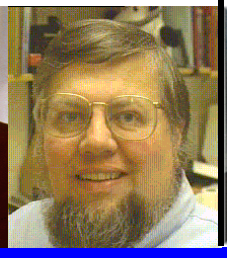
**1999**
- keynote: D. Tennenhouse, DARPA
- banquet: T. Sterling, JPL
- 1st banquet speaker

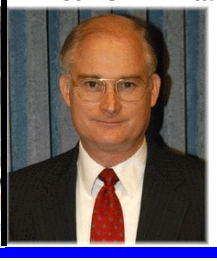
**2000**
- keynote: C. Holland, DUSD
- banquet: C. Williams, JPL
- 1st BAA/program announcement



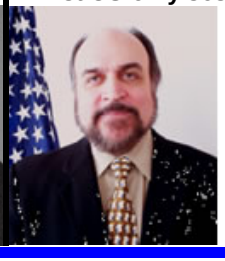

**2001**
- keynote: G. Bell, Microsoft
- banquet: T. Knight, MIT AI Lab
- 1st session dedicated to parallel MATLAB

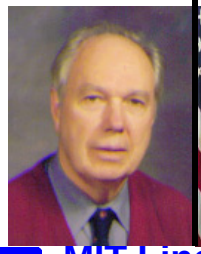
**2002**
- keynote: Maj Gen P Nielsen, USAF
- banquet: Cleve Moler, The Mathworks
- 1st VSIPL++ talk




**2003**
- keynote: J. Parmentola, ADRLM
- banquet: R. Kurzweil, Kurzweil Technologies
- 1st US-only session




**2004**
- keynote: D. Patterson, UC Berkeley
- banquet: M. Flynn, Stanford
- Grid computing

**2005**
- keynote: Brig Gen G. Connor, USAF
- banquet: M. Cusumano, MIT
- Cell processor


# Outline

- Big Picture Over Past Decade
- HPEC Representative Developments
- DoD Landscape and Impact on HPEC
- The Next Decade and Net-Centric Architectures
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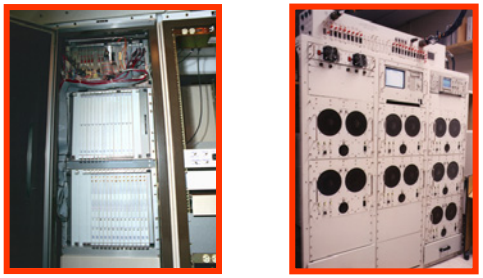
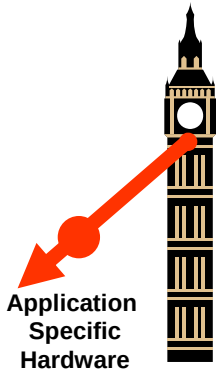
# A Decade of Embedded Computing

## Late 1980s - Early 1990s



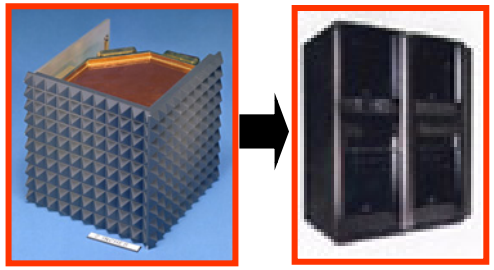


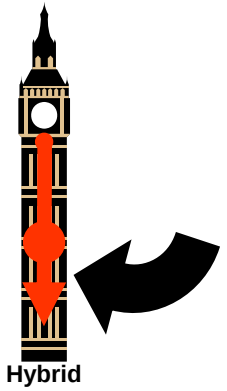

- Custom design
- COTS parts
- Non-portable SW
- Application specific prototype demonstration

## Mid-Late 1990s


- COTS HW
- Vendor specific SW
- Portable SW library
- Legacy SW
- June 1994- Sec. Def. Perry reduces reliance on military specs and standards: go commercial

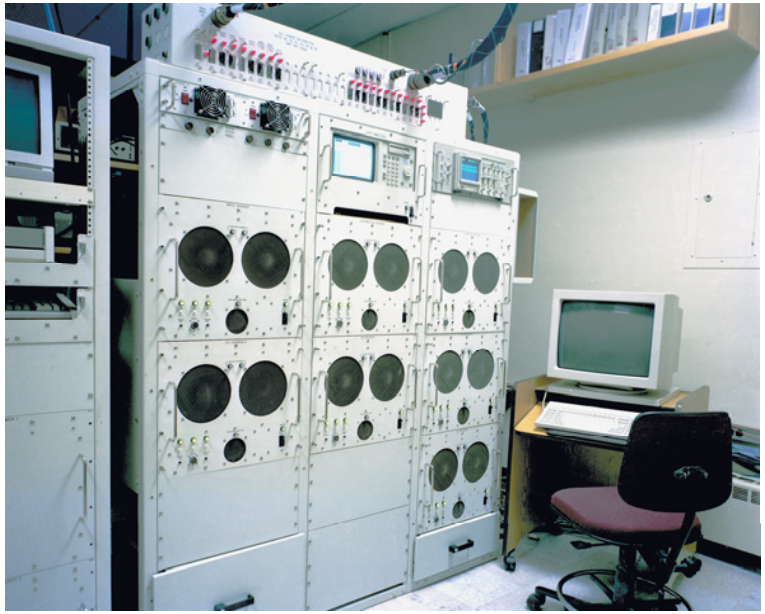
## Early 2000s - Mid 2000s






- Balanced architectures
- Custom front-end HW followed by COTS back-end
- SW standards
- Leverages information technology from commercial sector

# Early 90's Space-Time Adaptive Processor



## HARDWARE OVERALL COMPLEXITY

| COMPONENT TYPE | TOTAL SIZE |
|---|---|
| IC (LSI and VLSI) | ≈ 25,000 |
| UNIQUE CUSTOM BOARD DESIGNS | 13 BOARD DESIGNS<br>I/O 288 PINS<br>≈ 200 ICs<br>125 SQUARE INCHES |
| TOTAL BOARDS | 134 BOARDS<br>113 PRINTED CIRCUIT<br>21 WIRE WRAP |
| TOTAL CHASSIS | 14<br>11 REAL-TIME SIGNAL PROCESSING<br>3 CONTROL<br>21 SLOT 9U VME |

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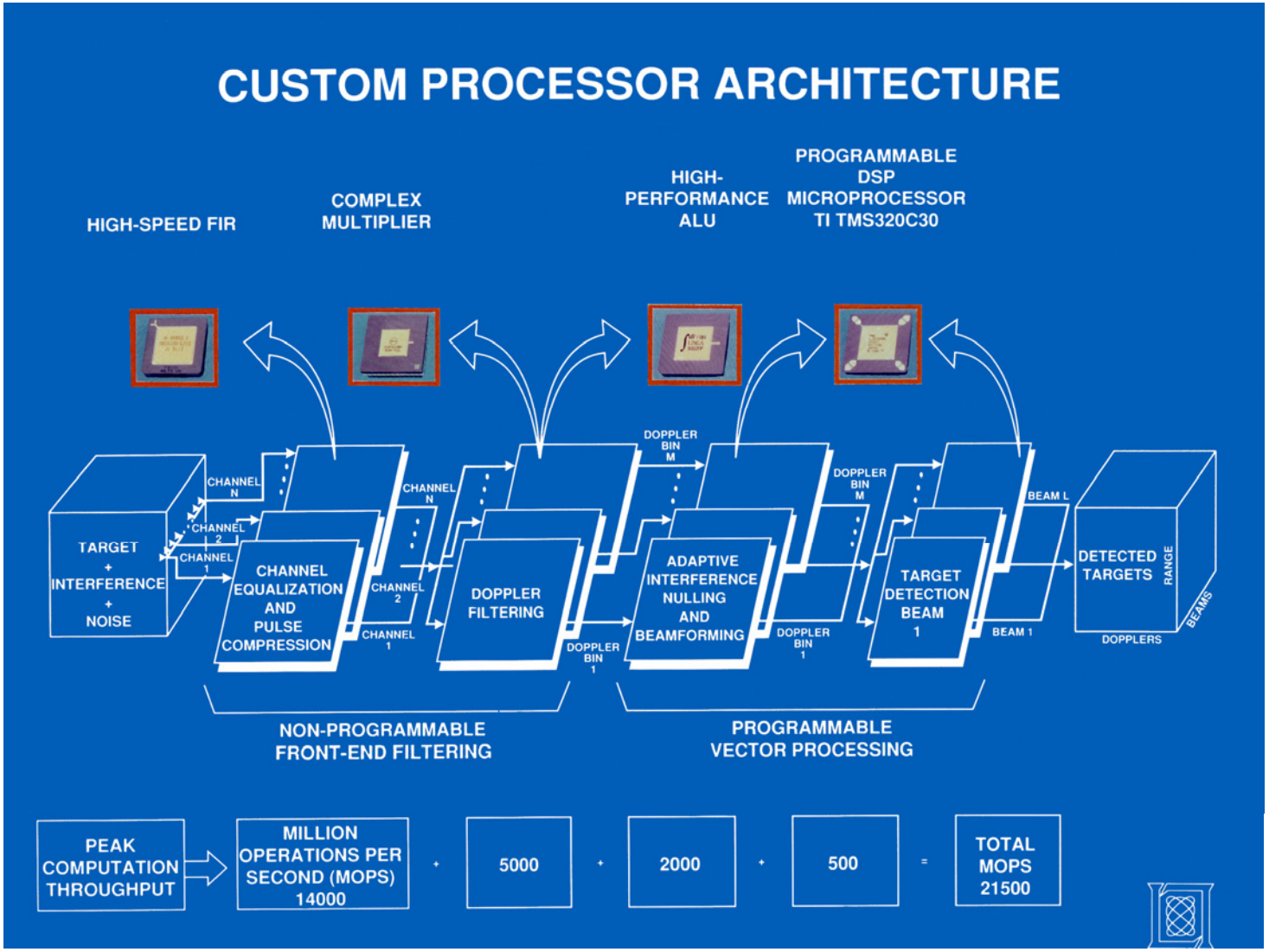
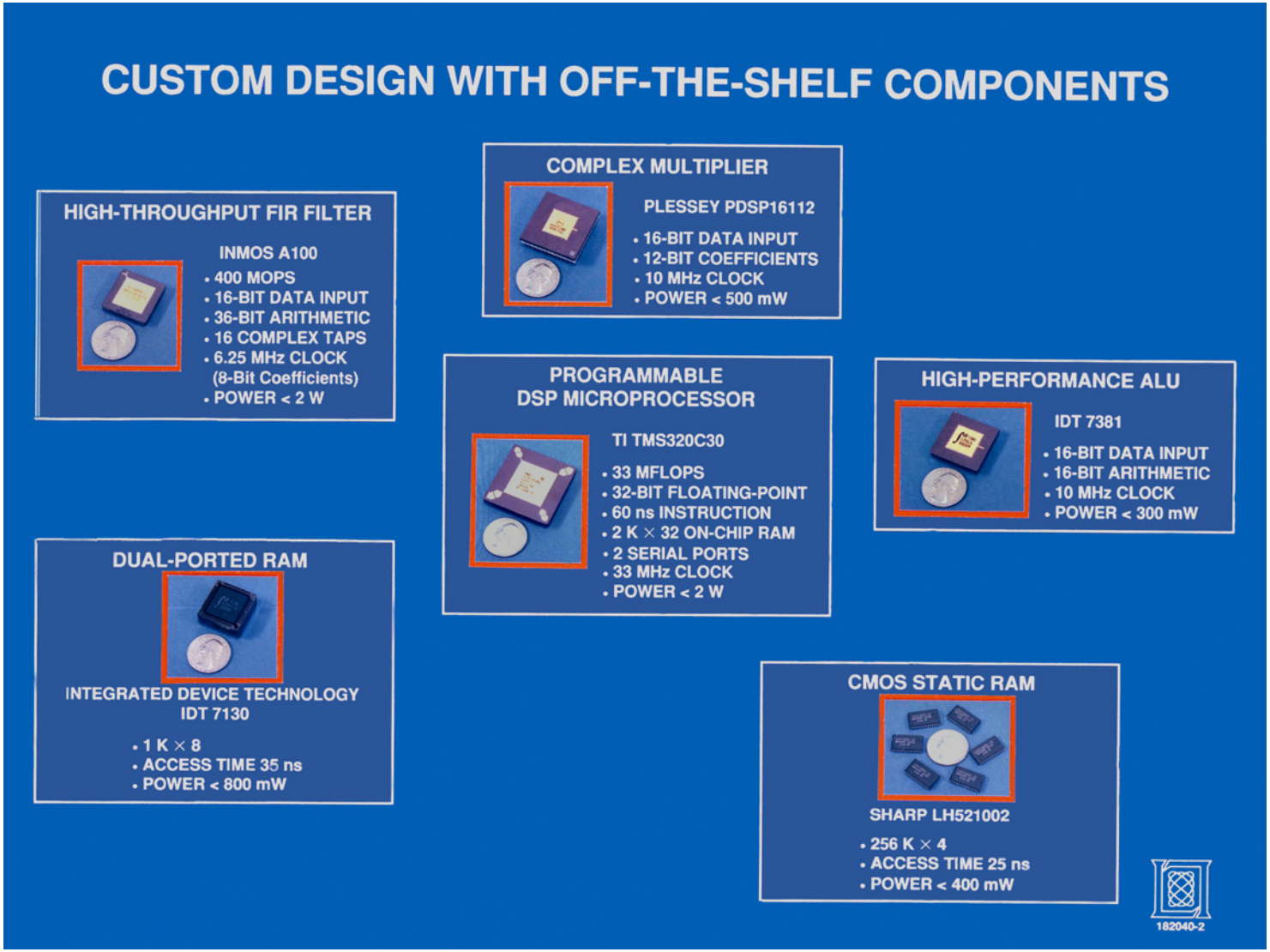
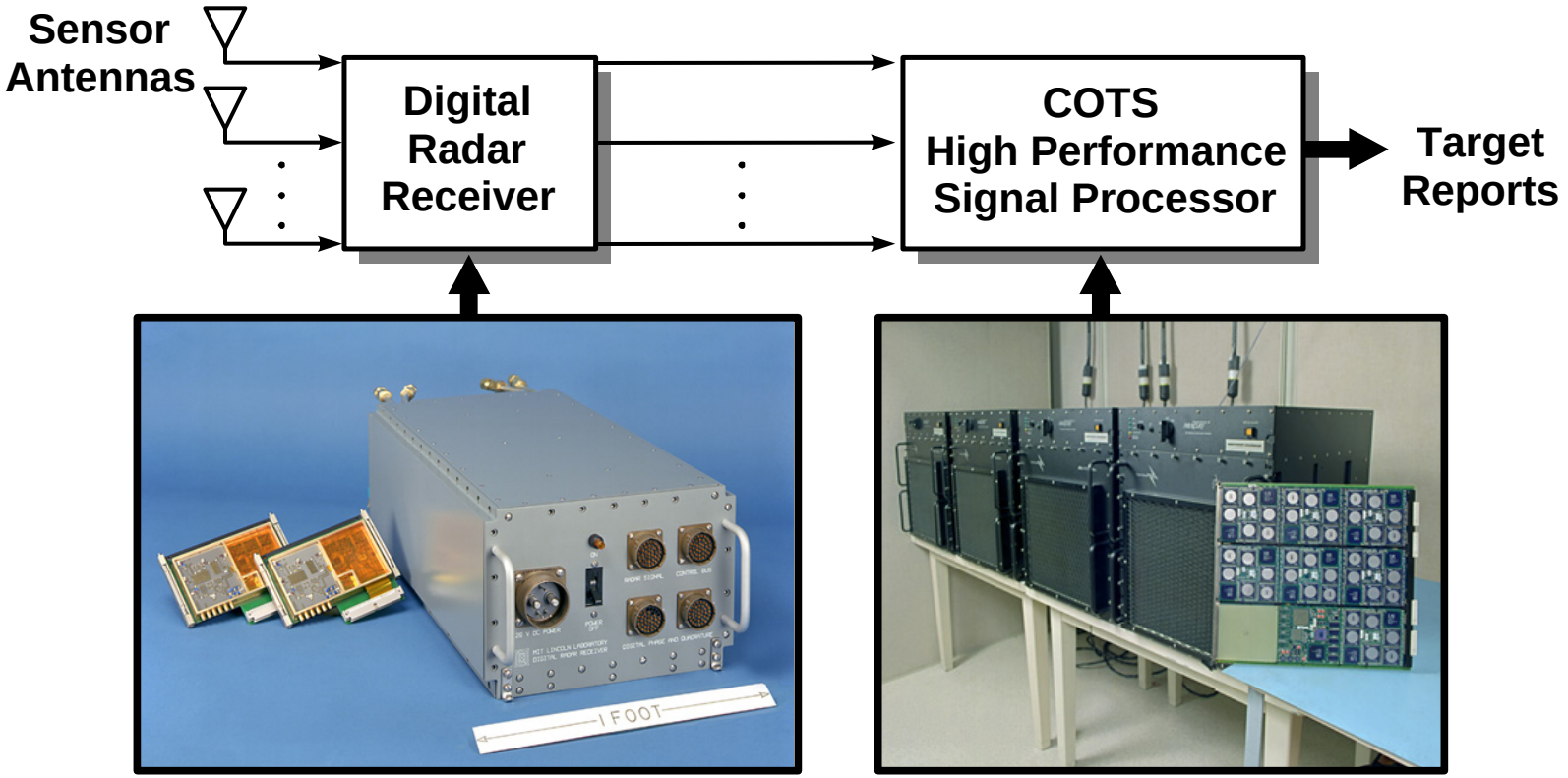
# STAP Processor Top Level Architecture



# Custom Design with COTS Components



# Embedded Real-Time Signal Processor




- Reduction in hardware size
- Flexible waveform design
- High performance digital filtering functions
- 100–1000 billion operations per second

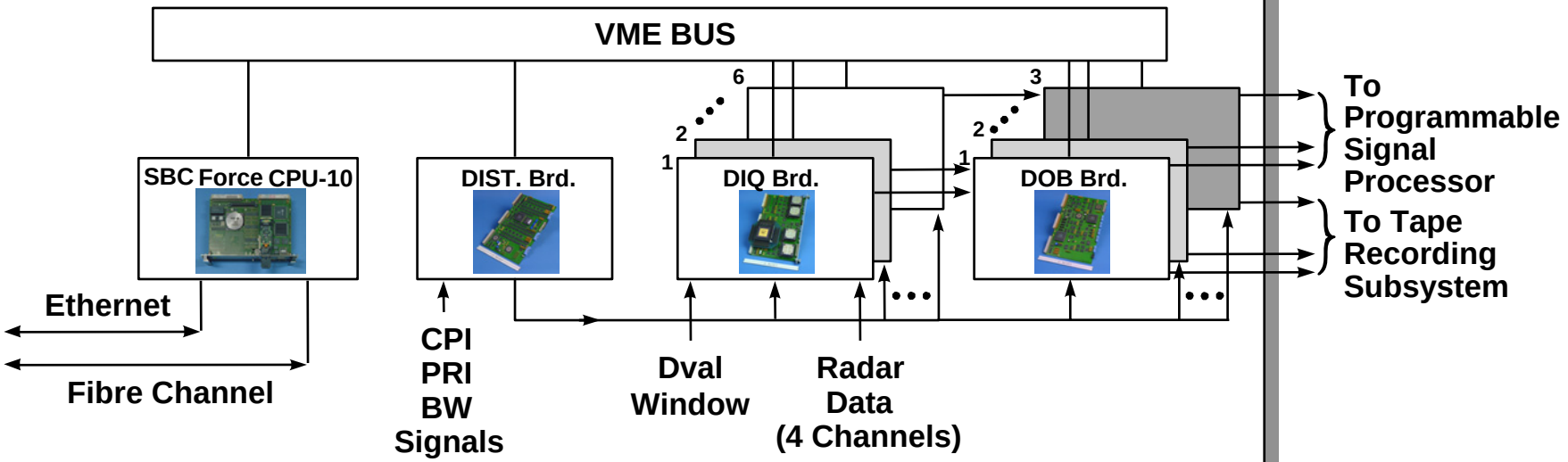
- Massively parallel processor
- Portable signal processing libraries
- Real-time performance
- 50–500 billion floating-point operations per second

# Front-End Processor Hardware

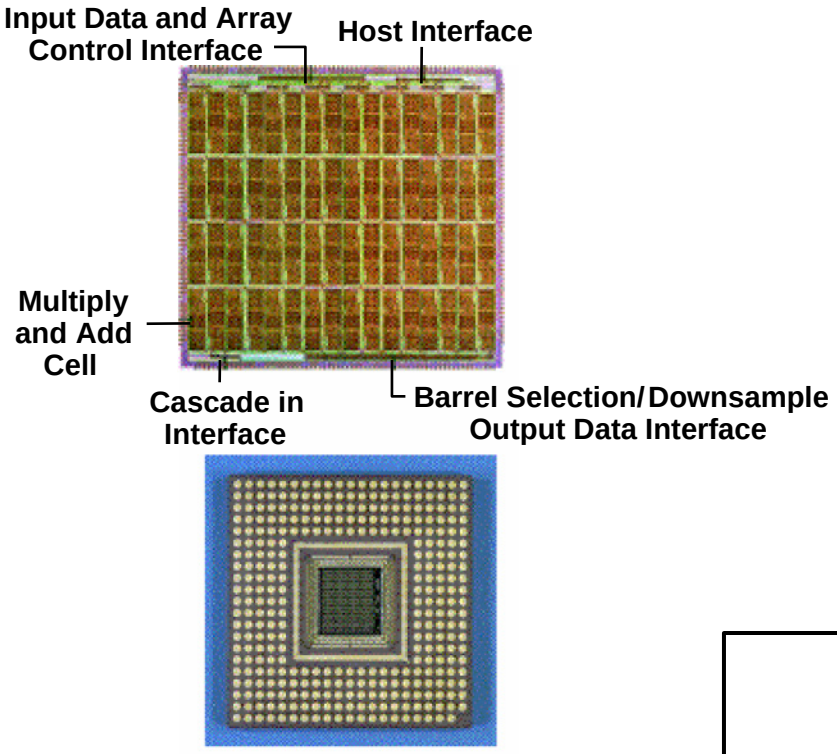

## Hardware Features

- Dedicated VLSI
- 100 GOPS
- Two 9U VME chassis
- Form factor:
  - 7.3 $ft^3$
  - 210 lbs
  - 1.5 kW
- Throughput density:
  - 14 $GOPS/ft^3$

## Chassis Level Architecture



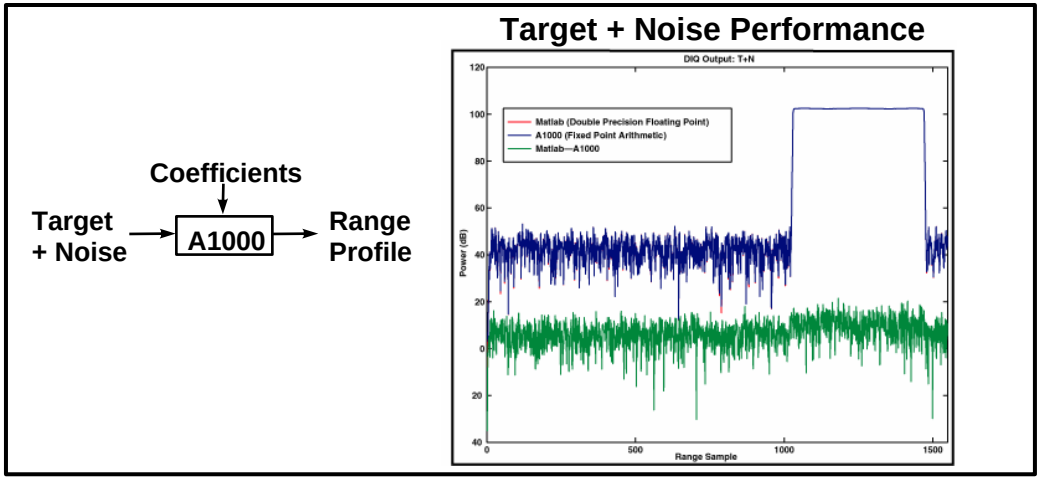
# VLSI Custom Front-End Chip



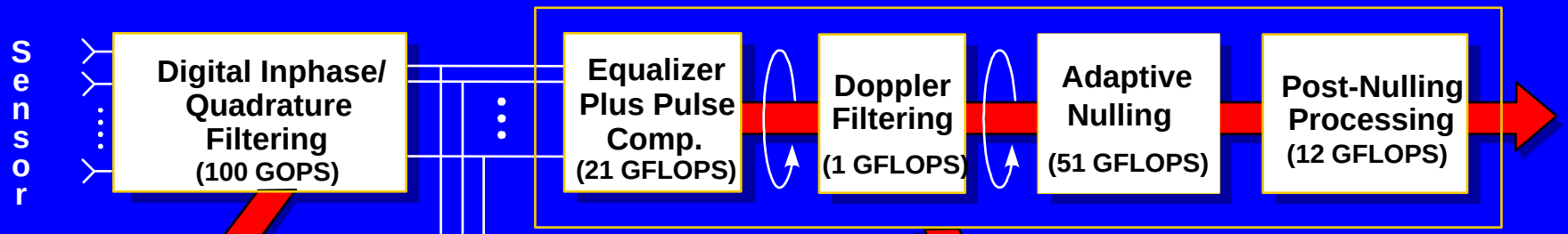

## ASIC Features

- 2 GOPS
- 585 mil x 585 mil die
- 1.5 Million transistors
- 0.65μ CMOS
  Three-layer metal
- 4 Watts/chip

## Performance Results



# Airborne Signal Processor




**Custom Hardware**

- Dedicated VLSI
- 100 GOPS
- Two chassis
- Form factor
  - 7.3ft$^3$
  - 210 lbs
  - 1.5 kW
- Throughput density = 14 GOPS/ft$^3$

**AMPEX Tape Recorder**

- Tape recorder rate = 30 Mbytes/sec
- 1 Bit error every 240 CPI
- 25 min cassette capacity
- Recorded data = 30% of available data with 17% waveform

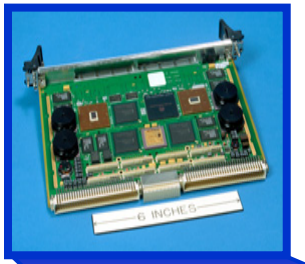
**COTS Programmable Signal Processor**

- SHARC AD21060 based
- 85 GFlops
- Bisection BW = 3.2 Gbytes/sec
- I/O throughput = 240 Mbytes/sec
- Four chassis
- Form factor
  - 33ft$^3$
  - 812 lbs
  - 6.9 kW
- Throughput density = 2.2 GFLOPS/ft$^3$

# Hardware Advances in Signal Processor Systems

200 GOPS
40 ft$^3$
1000 lbs
8.4 KW
22 MOPS/W

STAP Processor
1998



16 GFLOPS
< 1 ft$^3$
2 lbs
31 W
500 MFLOPS/W

Missile Seeker
2002

432 GFLOPS
46 ft$^3$
1200 lbs
7.2 KW
60 MFLOPS/W

Cluster
2005

1988 | 89 | 90 | 91 | 92 | 93 | 94 | 95 | 96 | 97 | 98 | 99 | 2000 | 01 | 02 | 03 | 04 | 05

Adaptive Processor
1992

22 GOPS
50 ft$^3$
1400 lbs
8 KW
3 MOPS/W

AEGIS Surveillance Radar
2000

43 GFLOPS
110 ft$^3$
1960 lbs
14 KW
3 MFLOPS/W

40 GFLOPS
7.5 ft$^3$
200 lbs
2 KW
20 MFLOPS/W

Knowledge Aided
Radar
2003

450 GFLOPS
9 ft$^3$
325 lbs
1.5 KW
300 MFLOPS/W

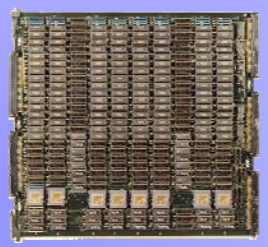
# Historical Perspective on Systems and Software

Capability

**Whirlwind**
SAGE
vacuum tubes
20 KOPS
assembly

**TX-2**
R&D
transistors
48-400 KOPS
assembly

**FDP**
DSP
transistors
5 MOPS
assembly



**SP-2**
DSP
custom / SIMD
760 MOPS
Fortran & assembly

**RAPTOR**
STAP
COTS
200 GOPS
C & assembly

**APT**
adaptive processing
22 GOPS
assembly & C

**KASSPER**
GMTI & SAR
COTS
480 GFLOPS
C++ & C

**Cluster Computing**
Advanced Signal Processing
COTS
432 GFLOPS
C++ & Linux

**Computational Throughput (1950 - 2003)**
20 KOPS to 480 GFLOPS
> Factor $10^7$ growth

1950s 1960s 1970s 1980s 1990s 2000s



FDP: Fast Digital Processor SP-2: Synchronous Processor 2

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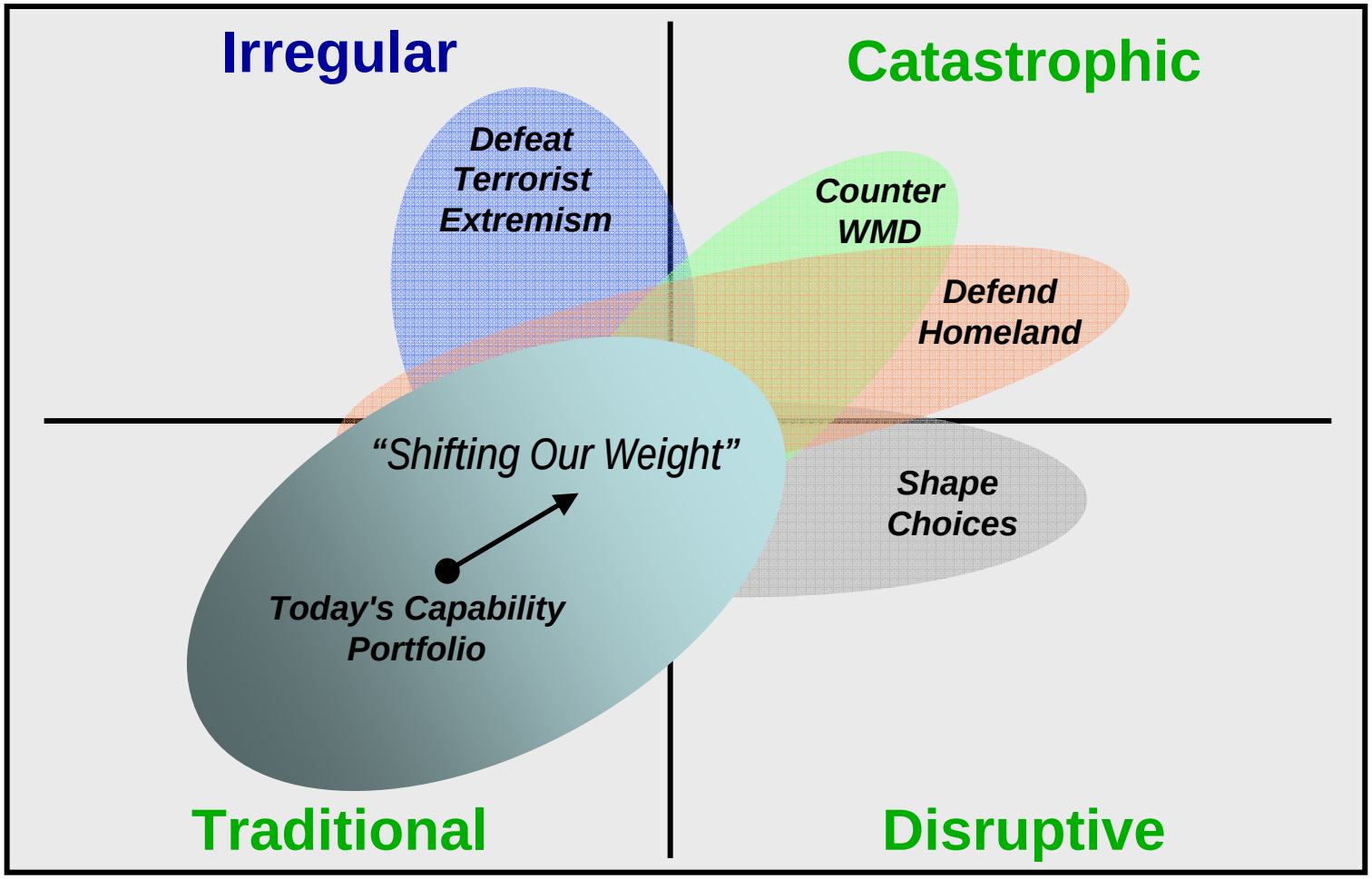
# DoD Quadrennial Defense Review




**Continuing the reorientation of military capabilities and implementing enterprise-wide reforms to ensure structures and process support the President and the warfighter**

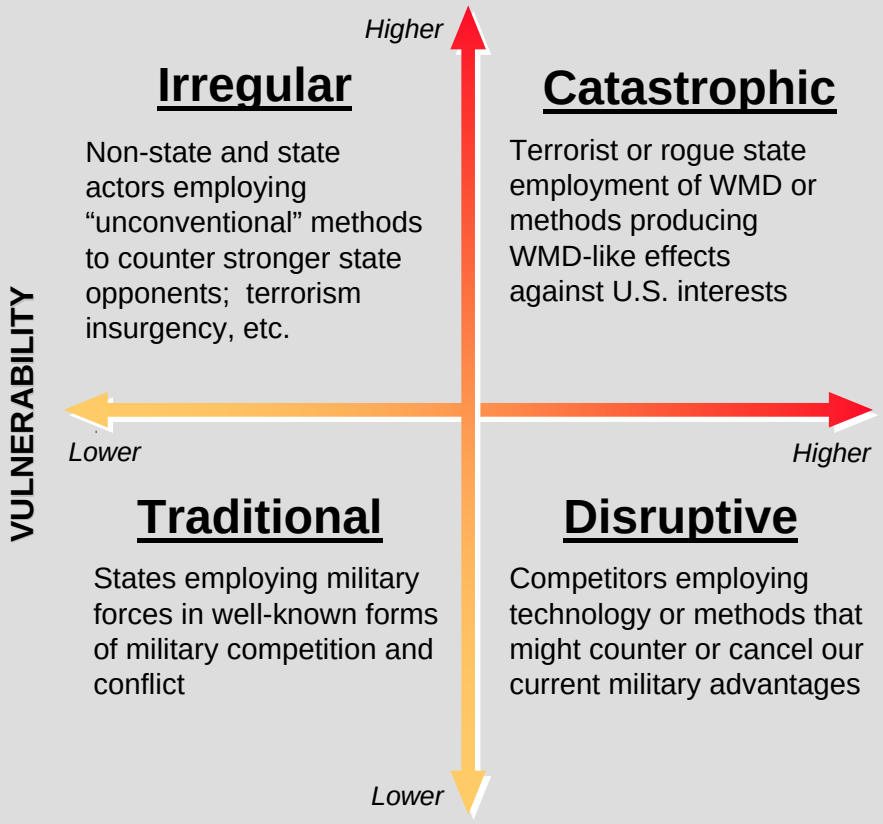


Note: From QDR Report, February 6, 2006

# DoD Options and Capabilities Provided

## Provide more options for President, capabilities for CoComs

### Post-9/11 Security Challenges




***Options for President***

***Capabilities for COCOMs***

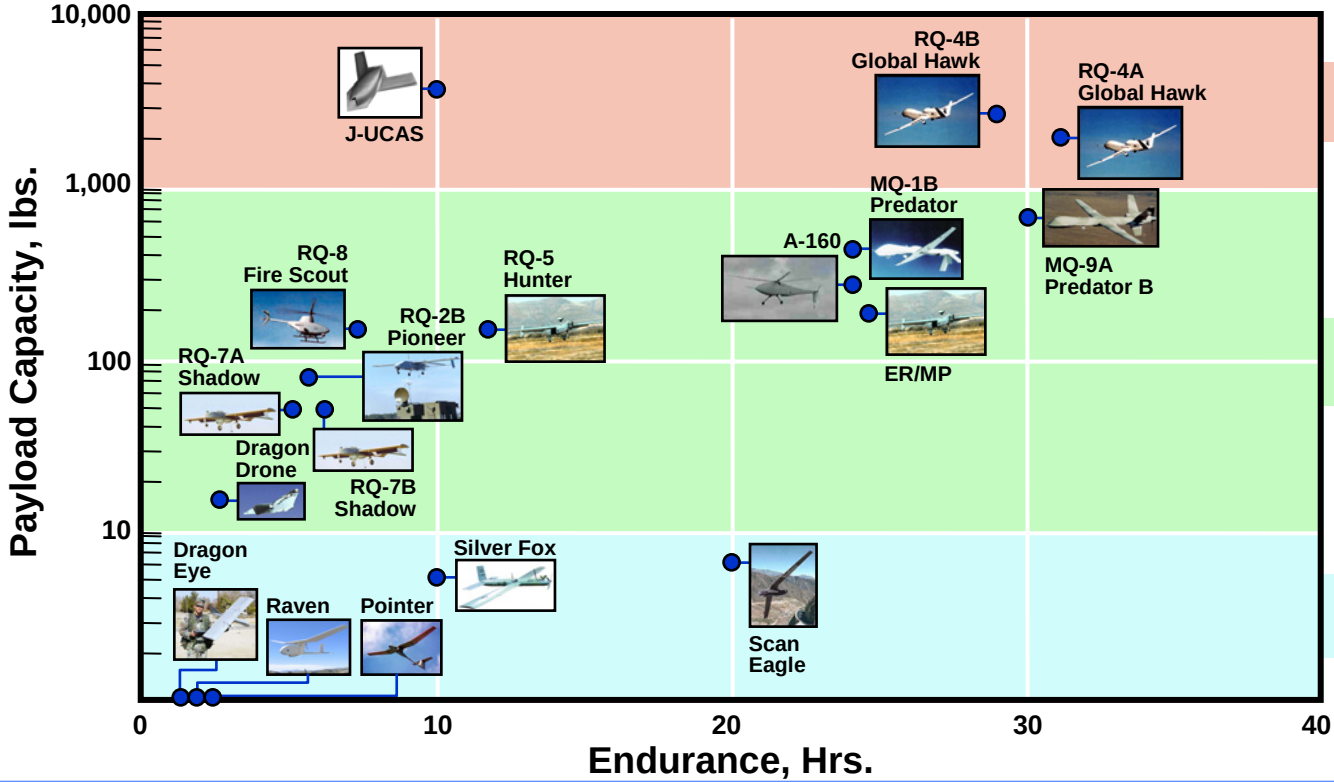
### Capability Focus Areas

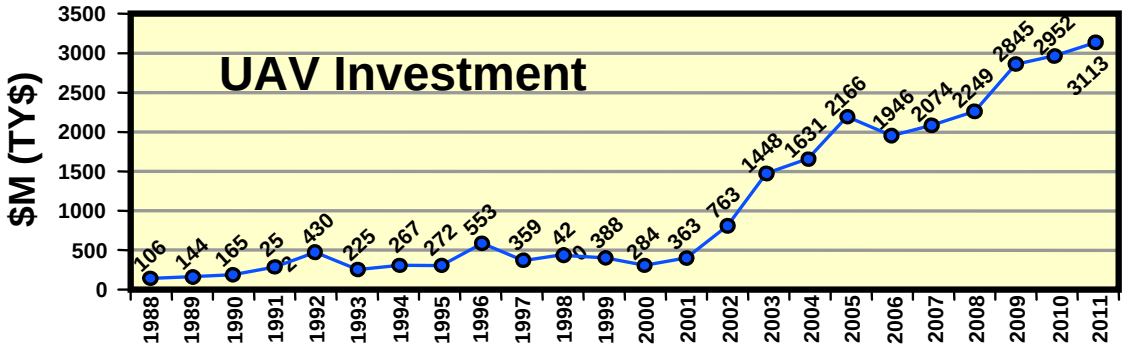
- **Defeat terrorist networks**
- **Defend homeland in depth**
- **Prevent acquisition or use of WMD**
- **Shape choices of countries at strategic crossroads** *(Assure, Dissuade, Deter, Defeat)*



**Note: From QDR Report, February 6, 2006**

# Growth in UAV Investment





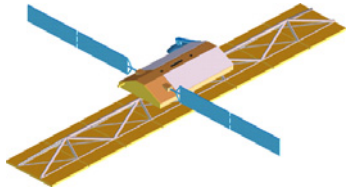

Note: Adapted from Unmanned Aircraft Systems Roadmap, 2005-2030.

# Next Generation Systems Employing Phased-Array Architectures

## Challenges Facing Next Generation Systems

- Multi-Function System Capability
  - Programming Flexibility
  - Rapid context switching
- Increase Number of Phase Centers
  - High Computation Throughput
  - High Comm. and Memory
- Very constrained in form factor
  - Small size, weight and power
- Open system architecture

*Space-Based Radar*



*JSTARS MPRTIP*


*Future Space-Based Radar*

*Navy Multi-Function Maritime Aircraft*

*Global Hawk MPRTIP*

*F-22*

*JSF DemVal*

*F/A-18 E/F*

*Navy Global Hawk*

# Functions-Platforms-Sensors Desired

## Functions

- Intelligence
- Surveillance
  - Space
  - Air
  - Ground
  - Ocean
  - Underwater
  - Subsurface
- Reconnaissance
- Targeting
- Monitoring
- Fire Control
- Guidance
- Communication
- Mapping
- Discrimination
- ATR
- Imaging
- BDA
- Command, Control
- Coordination
- Tasking
- ⋮

## Platforms

**Land**

Fixed sites, Vehicles
Personnel, UGS, UGVs

**AIR**

UAVs
(large, small, micro)
Aircraft, Aerostats,
Blimps,
Missiles, Shells

**Sea**

Ships,
Submarines
Underwater Sites,
UUV, Torpedoes

**Space**

Rockets
Missiles
Satellites

## Sensors

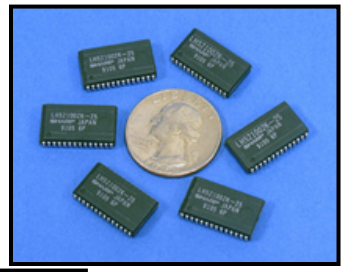
**Coherent Signal**

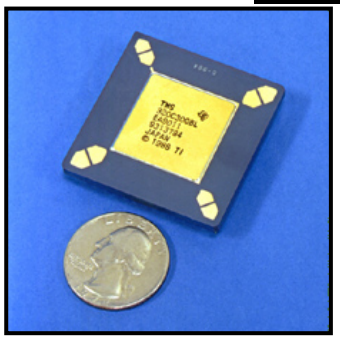
- Radar
  - SAR
  - MTI
- SIGINT
- Communication
  - RF
  - Laser
- Seismic
- Acoustic

**Non-Coherent Signal**

- Electro-optic
- Infrared
- Multispectral
- Hyperspectral
- Ultraspectral
- Nuclear/
- Chemical/
- Biological

# Trends in Computing Technology





## Memory

- Speed ↑ 7% / year
- ITRS* 2009 projections
  - 17 Gbits ($2^{34}$ bits)/chip
  - 50 nm half-pitch
  - 0.8 - 1.0 V
  - $223 / chip (1st year)

**Reference:* The International Technology Roadmap for Semiconductors (2005)

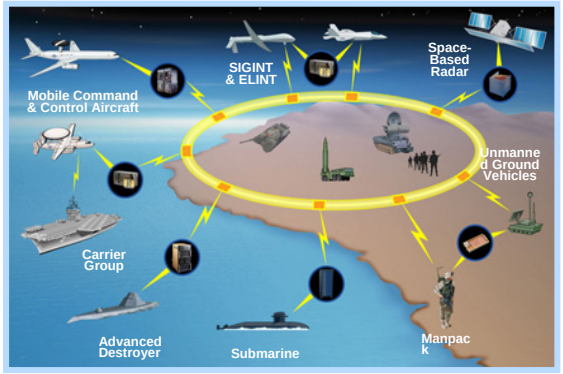
## Microprocessors

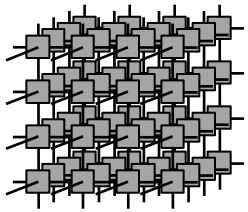
- ITRS* 2009 projections
  - Speed ↑ 60% / year
  - 773 M transistors
  - 52 nm half-pitch
  - 12 GHz clock speed
  - $85 / chip (1st year)

**Reference:* The International Technology Roadmap for Semiconductors (2005)

## System-of-Systems

*Warfare in the Littoral Environment*



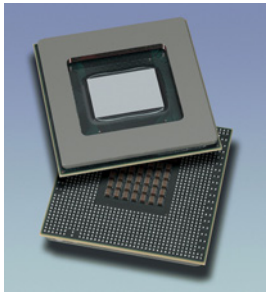
## System Interconnects

- Balanced architecture demands = 100s Gbytes for teraflops of computing
- Electrical based interconnects
  - Large power x volume product
  - Low performance for small message size transferred
  - Advances driven by commercial applications of network switching
- High-speed interconnects:
  - 10 Gbit Ethernet
  - 3GIO
  - HyperTransport / Infinipath
  - InfiniBand
  - Myrinet
  - QsNet
  - Rapid IO
  - SCI
  - StarFabric

*Reference:* Hot Interconnects Symposium
*Website:* www.hoti.org

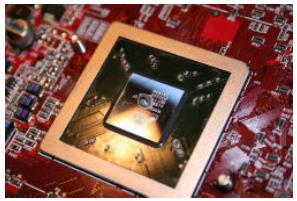
# Critical HPEC Enablers

## Cell Processor



- 3.2 GHz clock
- 200+ GFLOPS peak
- estimated 30-60 W

## Graphics / Video Processors




- ATI
- NVidia
- 550 MHz; 300 million transistors
- 256-512 bit memory bus
- 1-2 TOPS

## FPGAs



- Xilinx
  - 330K logic elements
  - 550 MHz clock
- Altera
  - 622 user I/O pins

## Chassis

- ATR
- VME / VME64 / VME64x

- air, conduction, or liquid cooling
- shock isolated vs. hard mounted

## Interconnects

- 10 Gbit Ethernet
- 3GIO
- HyperTransport / Infinipath
- InfiniBand
- Myrinet
- QsNet
- RapidIO
- SCI
- StarFabric

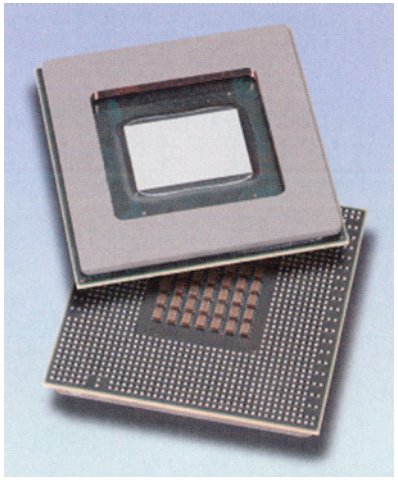
## Software

- VSIPL / VSIPL++
- MPI
- CORBA

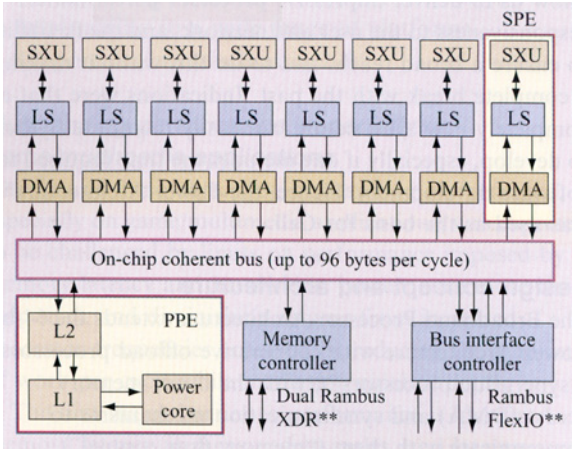
- VxWorks
- Linux / RT Linux

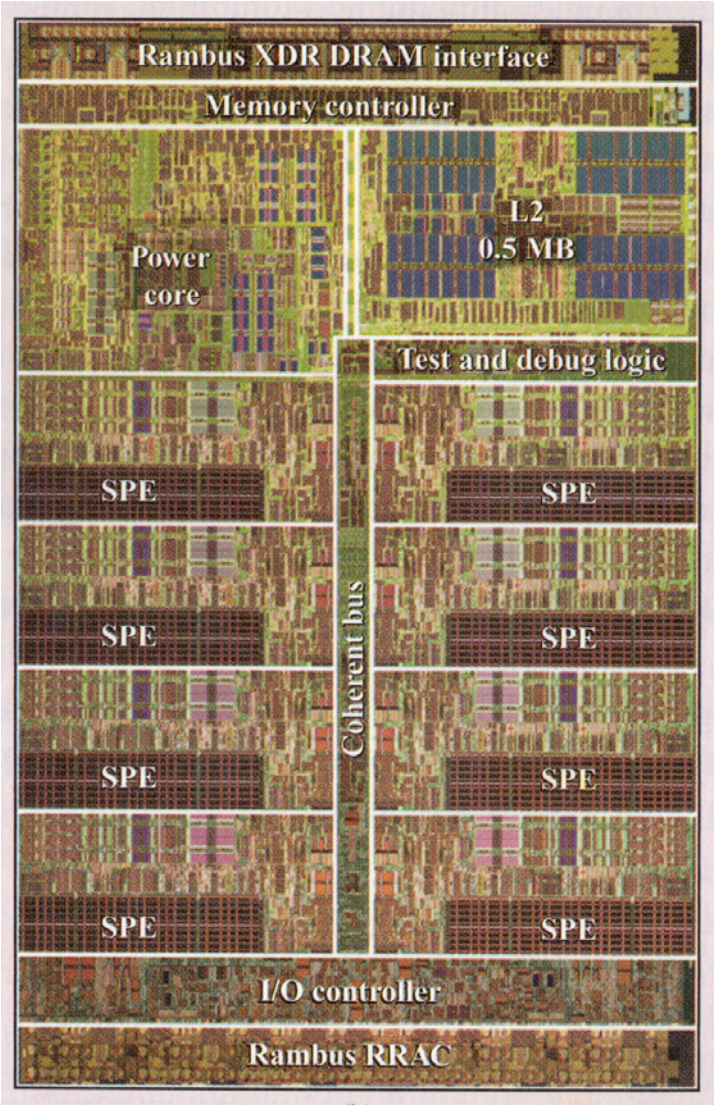
- Service-Oriented Architecture
  - XML
  - WSDL
  - SOAP
  - UDDI

# Cell Multi-Processor System



- Total peak performance over 200 GFLOPS running at 3.2 GHz
- 90 nm CMOS process
- 25.6 GBytes/sec to Rambus DRAM
- Up to 20 GBytes/sec communication bandwidth to graphics processor



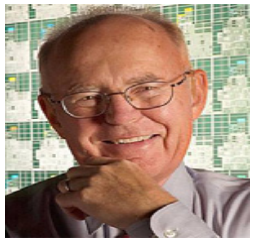




Reference: IBM Journal of Research and Development, Sept. 2005.

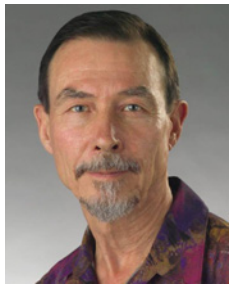
# Outline

- Big Picture Over Past Decade
- HPEC Representative Developments
- DoD Landscape and Impact on HPEC
- The Next Decade and Net-Centric Architectures
- Summary

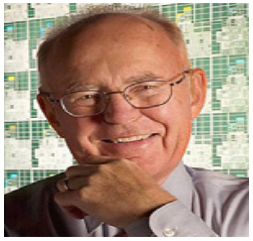
# Accuracy is more Important Than Precision when Projecting Forward



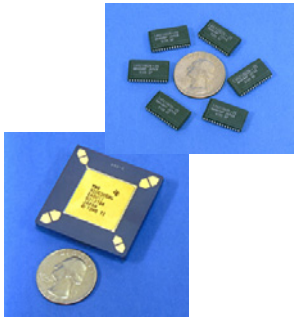
"Cramming More Components Onto Integrated Circuits," Dr. Gordon Moore Electronics Magazine, April 19, 1965 "2x/12 months"



Prof. Carver Mead Coins the Term "Moore's Law"



In 1975 Dr. Gordon Moore amends Original Statement to "2x/24 months"



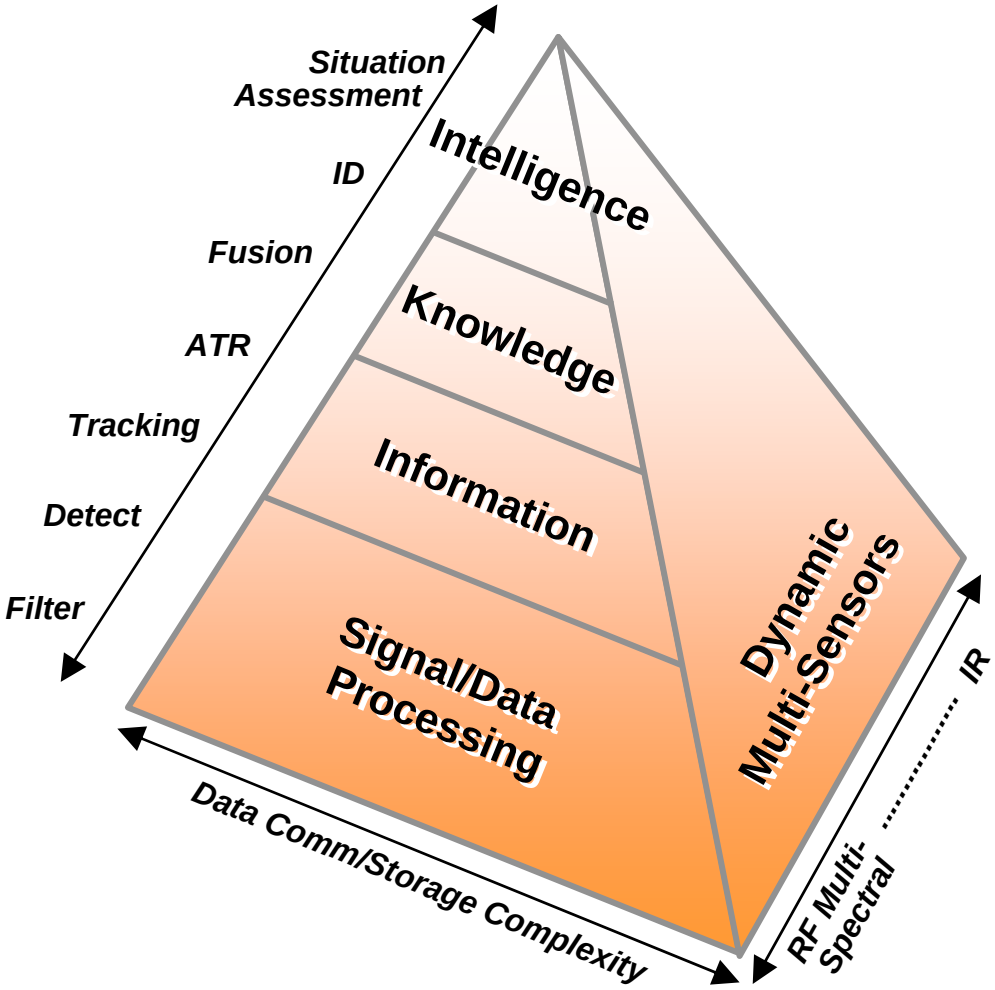
As Progress Continued Industry Modified Original Statement to "2x/18 months"

**Gordon Moore Recent Comments*:**

- "You know, engineers, we're always way too optimistic in the short run. But in the long run, it will evolve much further than we can see now."
- " I can never see more than about three generations…. The generation now is a couple of years….So I can see six to eight years further."

* Excerpt from: "Two pioneers Discuss Moore's Law and the Birth of an Industry," 40th Anniversary of Moore's Law, at the Computer History Museum, participants Dr. Gordon Moore and Dr. Carver Mead, Microprocessor Report Oct. 2005.

# HPEC Spanning a Broader Spectrum of Application




Note: Spectrum of applications credited to Bob Graybill, DARPA PCA Program.

# Changes in Force Structure*

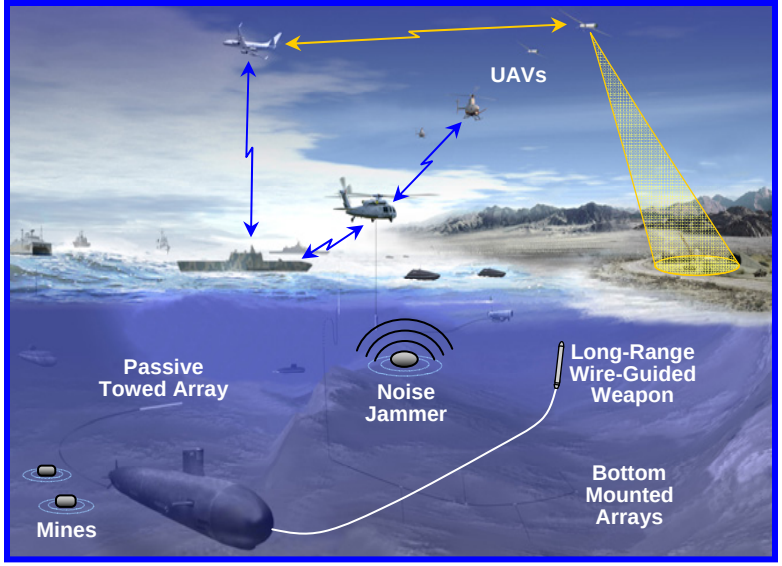
## - Navy Example -

### Today

**Platform-Centric**

### Tomorrow

**Network-Centric**




Evolving

- Stove-pipes
- Limited flexibility to adapt to new missions
- Large foot-print

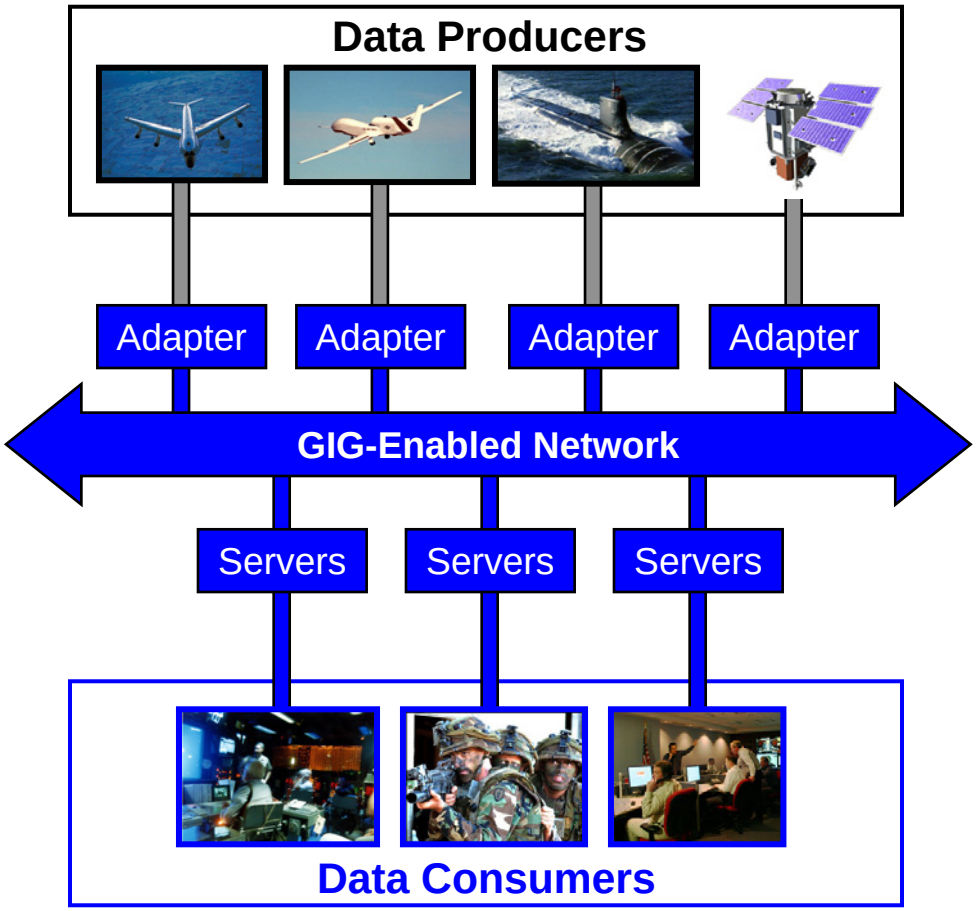
- Network-based vs. hub and spoke model
- Global connectivity and continuous information sharing
- Expeditionary forces



* Extracted from C4ISR for Future Naval Strike Groups, National Research Council

# Migrating to a Net-Centric Architecture

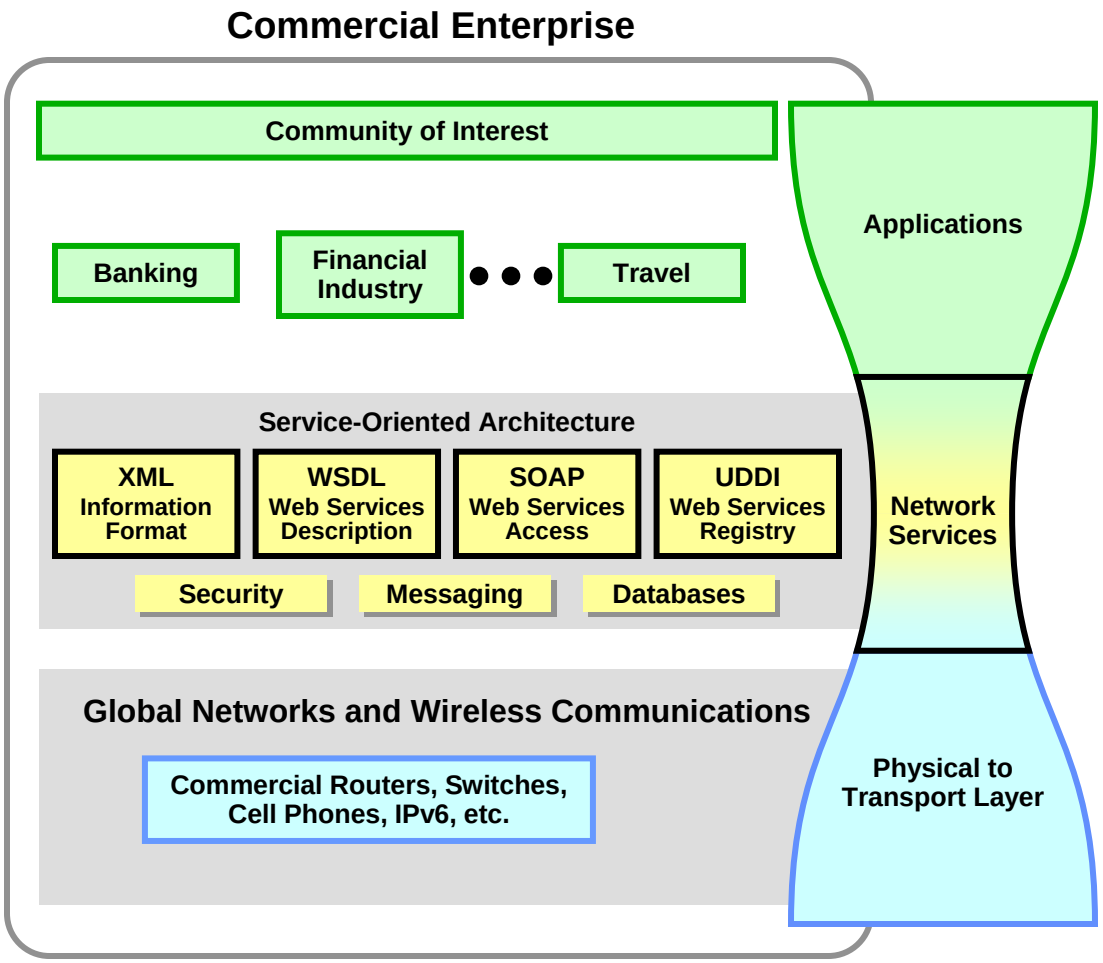
## Global Information Sharing




## Net-Centric Technologies

- Commercial sector
  - Service oriented architectures
  - Web services
  - Terrestrial and wireless comms
  - Semantic Web
- Military sector
  - Global Information Grid
    - GIG-Bandwidth Expansion (terrestrial)
    - Joint Tactical Radio System
    - Transformational Satellite (TSAT)
    - Network Centric Enterprise Services (Core enterprise services to the GIG)
    - Information Assurance (encryption)
    - Teleport (theater, reach-back)
    - Joint network management system (joint network management tools)

# Building from a Commercial Service-Oriented Architecture

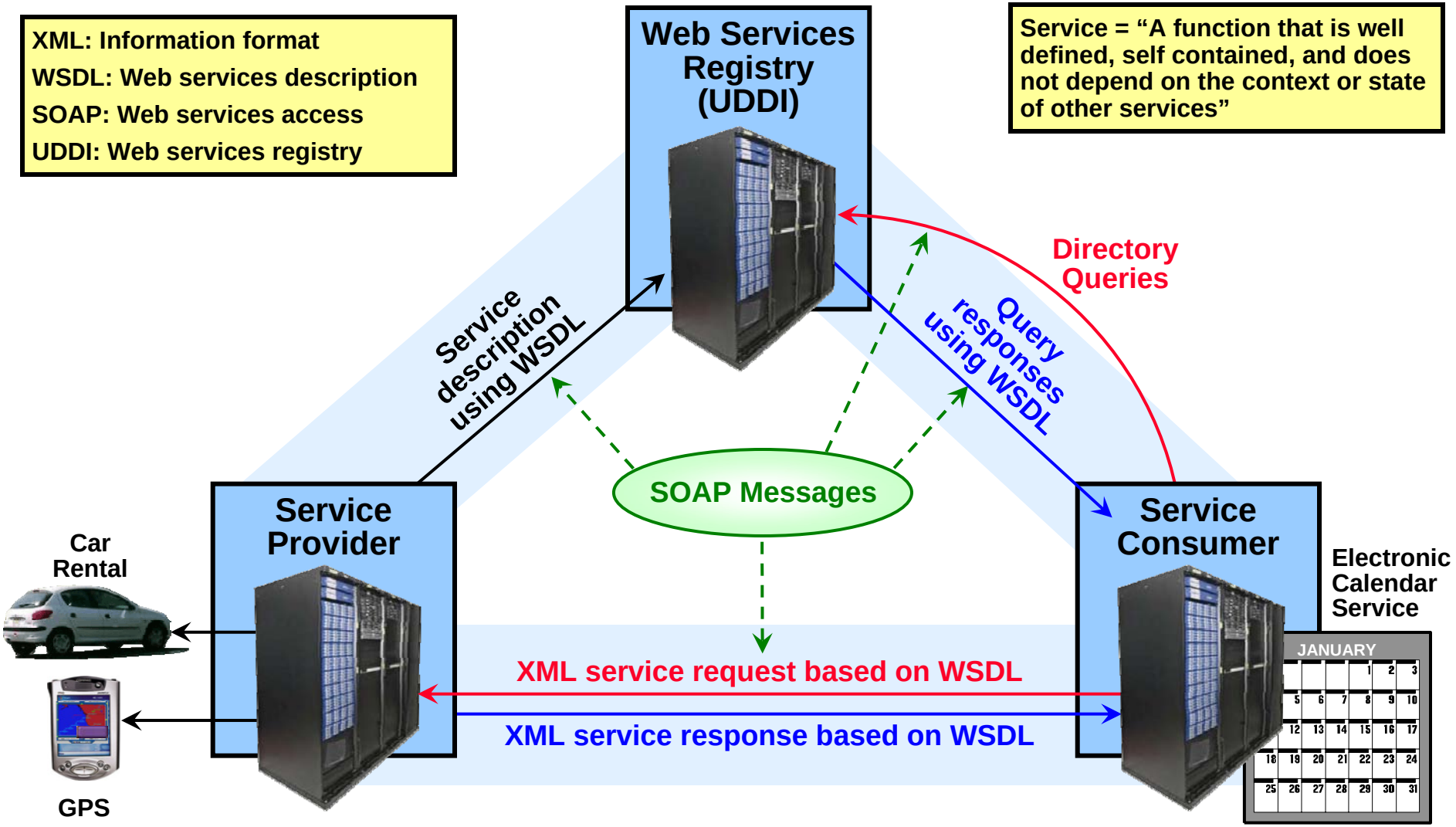



* NCES = Net-Centric Enterprise Services
* HAIPE = High Assurance IP Encryption Hardware
* GIG = Global Information Grid

# Web Services Basics*

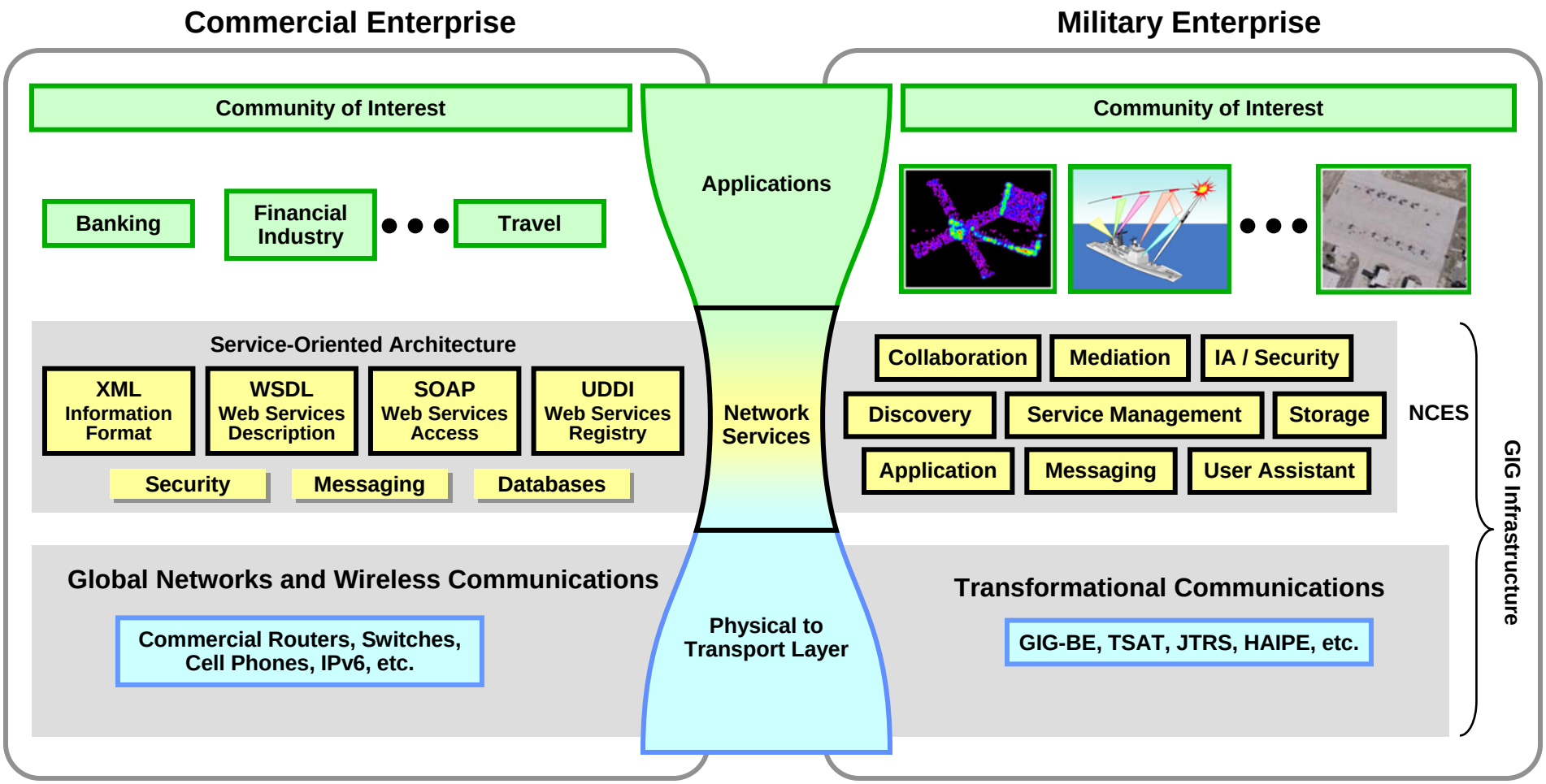
XML: Information format
WSDL: Web services description
SOAP: Web services access
UDDI: Web services registry

Service = "A function that is well defined, self contained, and does not depend on the context or state of other services"




* From Web Services and Service-Oriented Architectures, D. K. Barry, 2003

# Building from a Commercial Service-Oriented Architecture




* NCES = Net-Centric Enterprise Services
* HAIPE = High Assurance IP Encryption Hardware
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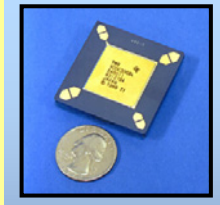
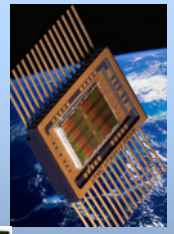
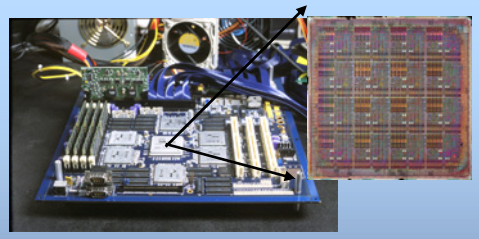
# HPEC Opportunities

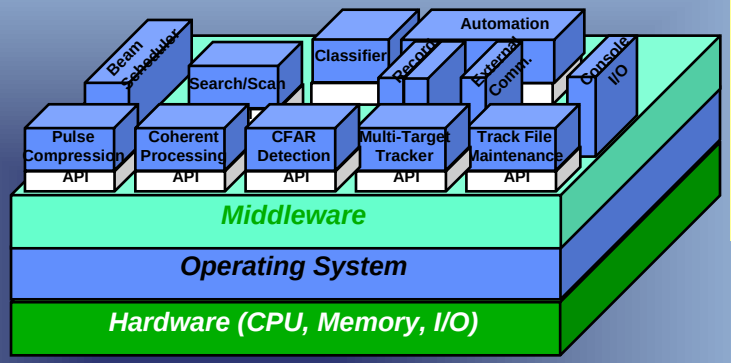
## Advanced HW

- FPGAs, Standard Cell ASICs for high-performance front-end sensor processing
- Mixed circuit & custom VLSI at the sensor extreme front-end










## Programmable Processors

- GPUs, Cell, Clearspeed, PCAs
- Rad tolerance
- Low power
- Anti-tamper

## Development Tools

- Co-design, co-development of hybrid processors
- Model-driven architectures
- Rapid-prototyping tools

## Systems

- Smart sensors with knowledge-based processing
- Service-oriented sensors
- Collaborative HPEC in scalable networks
- Multi-function, multi-modal agility

## Software

- Runtime environments for hybrid systems
- Intelligent middleware for on-line optimization
- Middleware for GPUs, PCAs, Cell,…

# Summary

- High performance embedded computing has gone through a significant evolution over the last 15 years
  - Started as a principally a custom-based set of solutions
  - The evolution forced a more COTS-based solution
  - Meeting today's requirements demands a hybrid solution
- The new set of conflicts (e.g. GWOT) is demanding much rapid deployment cycle
  - Enemy changes tactics too fast compared to our acquisition cycle
- The DoD landscape will continue to demand significant embedded computing capabilities
  - A wide spectrum of solutions are available ranging from programmable processors, rapidly reconfigurable FPGAs, to custom VLSI designs
- One emerging area is in distributed computing in support of net-centric architectures
  - Many TeraOps in computation
  - Distributed memory and archiving
  - Fast I/O and interconnects