

# Field Programmable Multi-Cores: A New Class of Semiconductors

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## Introduction

There are two major trends in the High Performance Embedded Computing market; the drive for lower size, weight and power (SWAP) and the push for ever increasing levels of computational performance. The scaling of transistors to provide ever faster microprocessors through higher clock frequency is coming to an end [1]. Performance increases are relying on multi-core processing going forward. Another trend is the need for flexibility in order to accommodate changing requirements in the field. Further complicating the issue are the considerable number of legacy systems with large amounts of proven, critical software that need to be affordably modernized to meet future demands. This is particularly true for the military portion of the market. At first glance, these trends appear to be at odds with each other. However, recent advances in System-on-Chip and interconnect technology, combined with electronic system-level design tools have fostered the development of a new class of semiconductors, called Field Programmable Multi-Cores, that address these requirements.

## Field Programmable Multi-Cores (FPMCs)

Combining the flexibility of Field Programmable Gate Arrays (FPGAs) with the density, speed and low power of System-on-Chip (SoC), the Acalis™ family of Field Programmable Multi-Cores (FPMCs) is a sea of cores combined with a Programmable Interconnect Fabric™ (PIF) that can be configured in the field. As shown in Figure 1, the cores are a combination of processor units, I/O processors, RAM memories, memory controllers, general logic, general I/O, and PIF connection units. The exact type of cores and the number of each depends on the specific family member. Acalis devices facilitate the migration of microprocessor based systems to multi-core computing, while uniquely preserving the investment in existing software.

Developed in collaboration with IBM, the Acalis FPMCs are being fabricated at the Trusted Foundry. The combination of known Intellectual Property (IP), SOC development tools, and trusted manufacturing source provides the highest level of assurance.

These FPMCs provide a method for developers to quickly configure a SoC for their system. The proven cores and PIF eliminate the risk in developing the SOC. The available silicon eliminates the time and high cost of fabricating silicon.

Multiple Acalis FPMCs can be used in a given system and they are architected to readily interface to FPGAs to provide the maximum flexibility for a system.

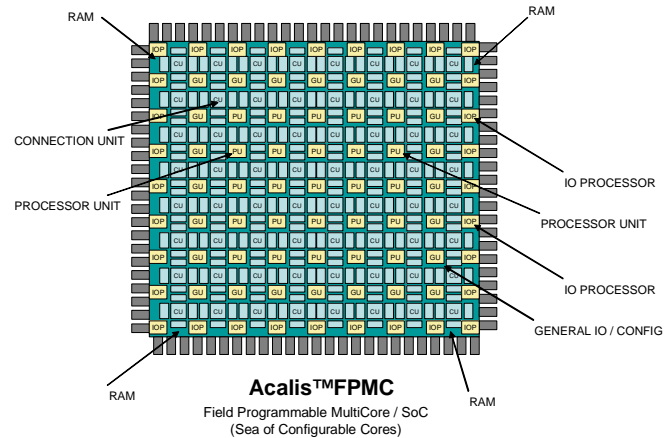


Figure 1: Acalis™ Field Programmable Multi-Cores.

In order to minimize power, all cores start in standby mode until they are enabled so the FPMC hardware can be configured and adapted to meet the needs of the system.

A suite of design tools, called the SystemLab™ Integration Station, contain the advanced tools needed to generate the configuration file and to program the numerous heterogeneous processor cores. A simulator for the Acalis family is also available. These tools provide a high level of control and visibility of the multi-processing chip. Figure 2 shows two SystemLab screens. The rear one contains a multi-core simulation and the front one displays the contents of three distinct memories. Both screens show different types of instrumentation, including performance bars.

## Acalis™ FPMC Applications

There are two distinct groups within the Acalis family. The first group is designed specifically for compatible integration and performance. Part of the cores are advanced IP and part of the cores are legacy IP. Different family members offer different software compatible core combinations.

By preserving the existing software, Acalis FPMCs provide a quick and cost effective migration path from legacy microprocessor systems to state-of-the-art multi-core. They can directly execute unmodified legacy software and

simultaneously execute IBM PowerPC® multi-core software on a single chip device. The legacy software can remain on the legacy core or it can be ported to the advanced IP over time as funding and resources become available.



**Figure 2: SystemLab™ Integration Station**

The second group is designed for scalable performance. Each chip is essentially a multi-core computing node on a chip. The exact offering depends on the family member. These parts can work either as an extension to an existing system or as a stand-alone computer.

At only 3.7 System Watts/GFlops, taking into account all of the memories, processors, routers, interfaces, etc., they are ideal for battery powered or other power conscience systems. For comparison, the most optimal personal computer dissipates 70 System Watts/GFlops.

Their high level of integration make them a good fit for space and weight constricted systems. For example, sixty-four general purpose processors and floating point processors with I/O processors, interfaces and substantial memory subsystem fit within a space that is approximately four square inches.

## Summary

Field Programmable Multi-Cores (FPMCs) are a new class of semiconductors that offers the flexibility and low development cost of FPGAs and the high density, low power and high performance of SoCs. Acalis FPMCs offer a sea of cores combined with a Programmable Interconnect Fabric™ (PIF) that can be configured in the field. They facilitate the transition to multi-core systems by providing software compatibility with existing and legacy systems. Scalable high performance is also available with parts that offer a balanced computer node on a chip. The SystemLab™ Integration Station provides the advanced design tools needed to generate the configuration file and to program the various processor cores. The Acalis family is applicable to a broad range of general purpose and embedded computing systems.

## References

- [1] Sperling, E. (2005, March 4). The Sum Is Greater Than the Whole. *Electronic News*. Retrieved March 8, 2005, from <http://www.reed-electronics.com>.