VSIPL++
HPEC Kernel Benchmarks

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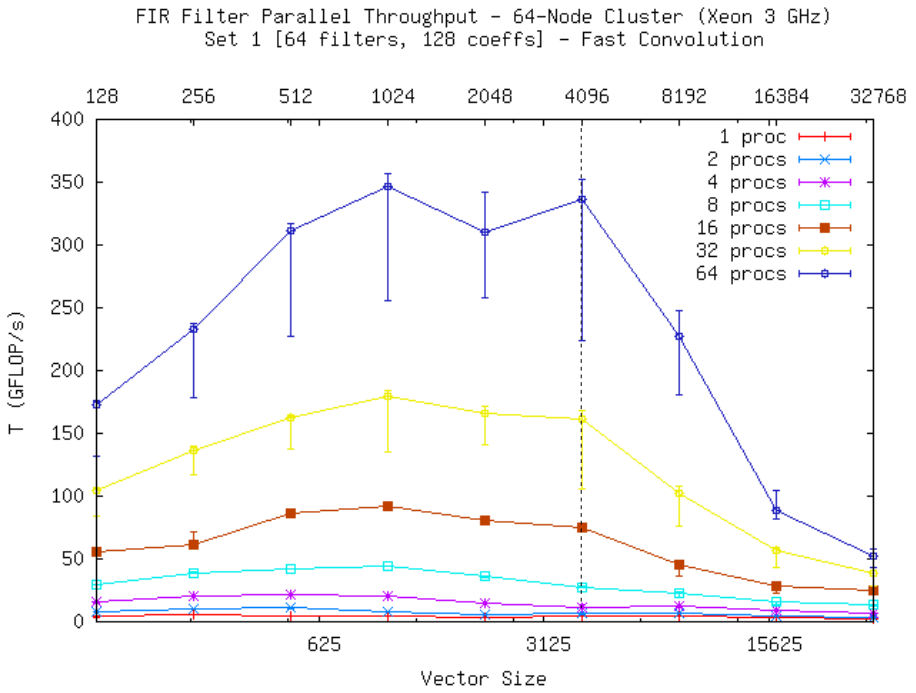
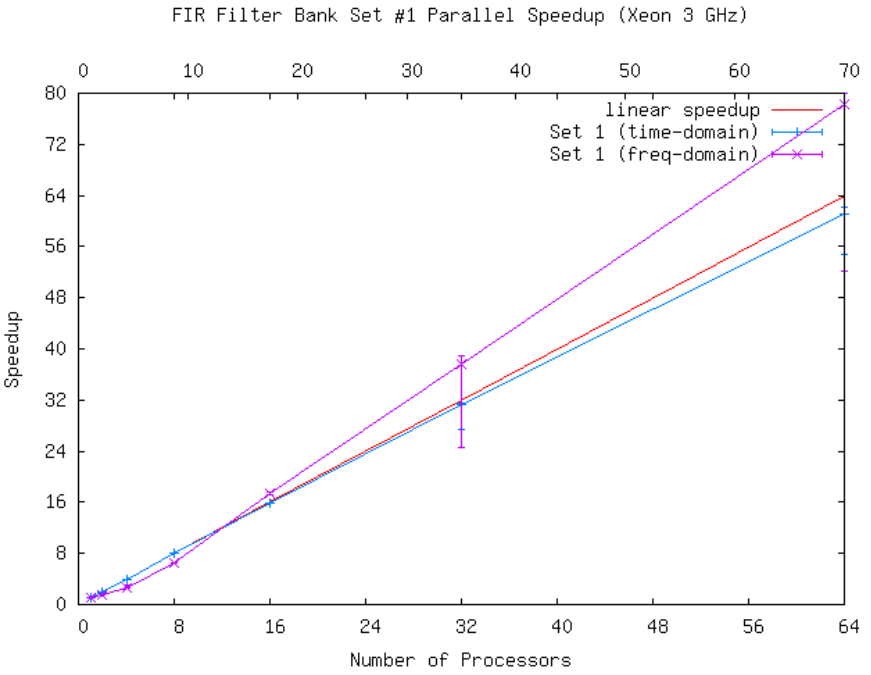
Jules Bergmann, Don McCoy,
Assem Salama, Stefan Seefeld
CodeSourcery
{jules, don, assem, stefan}@codesourcery.com
888-776-0262

Sourcery VSIPL++ Advantages:

- **Productivity**
  - SIP algorithms can be implemented efficiently and effectively
  - Parallel version of code implemented with few changes to serial version
- **Performance**
  - Utilizes vendor libraries for good performance with low overhead
  - Throughput is nearly the same as the serial version
  - Achieves expected linear speedups for parallel versions
- **Portability**
  - Identical code runs on all supported systems.
  - Reconfigurable to use vendor libraries optimized for a given system
- **Parallelism**
  - Minimal code changes
  - No MPI programming
  - Near-zero performance overhead in serial case

FIR Bank: Serial vs Parallel





Data Set #1 – Fast Convolution

- Run on 64 Xeon processors
- Speedups shown for 4096 points

Data Set #2

- Shows similar speedups

CPUs	GFLOP/s	Speedup
1	4.3	1.0
2	6.3	1.5
4	10.9	2.5
8	27.8	6.5
16	75.1	17.5
32	161.9	37.7
64	**336.8**	78.3