

Benchmark Results for Ultra-High Performance Scalable Processing Architecture for Embedded Signal and Image Processing Applications

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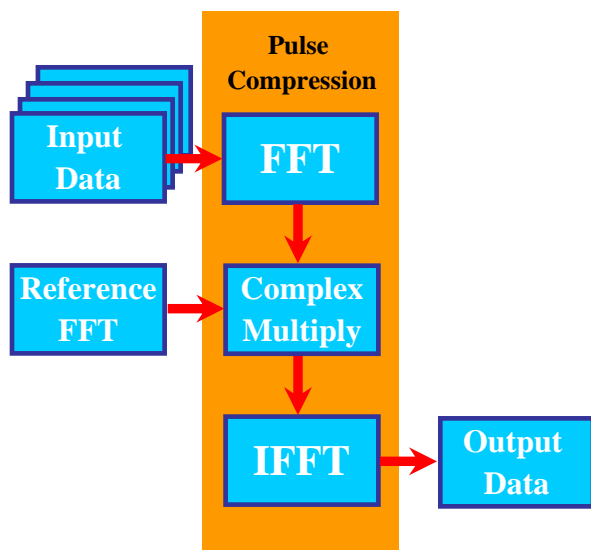
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1024-point complex Pulse Compression

■ *Per chip measurements:*



- 96 PE's enable 12 sets in parallel
 - 8 PE's per PC
- 9.39 usec DRAM to DRAM
- 9.87 usec on-chip (ie without I/O from/to DRAM)
- 11.55 GFLOPS with I/O
- 11.02 GFLOPS without I/O

Overlapping of I/O and compute results in **95%** of cycles being used for computation

Pulse Compression Demonstration

Hardware Performance



Routine	Buffer (12 signals)	1K signal	Time	Rate (signals/sec)
FFT	12.7K cycles	1.06K cycles	4.23 usec	236K (fft only)
CM	2.2K cycles	0.18K cycles	0.73 usec	-
IFFT	13.3K cycles	1.11K cycles	4.43 usec	226K (ifft only)
Filter work	28.2K cycles	2.35K cycles	9.4 usec	106K (no I/O)
DRAM_READ	0.7K cycles	0.06K cycles	0.23 usec	-
DRAM_WRITE	0.7K cycles	0.06K cycles	0.23 usec	-
TOTAL	29.6K cycles	2.47K cycles	9.87 usec	101K PC/sec per chip

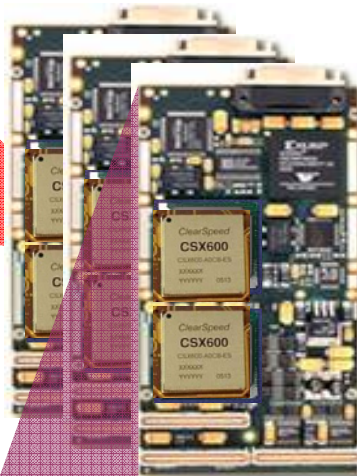
Best in World!!



Scalable Processing Platform™



~100 GFLOPS
64-bit FP
PMC/XMC Daughtercard

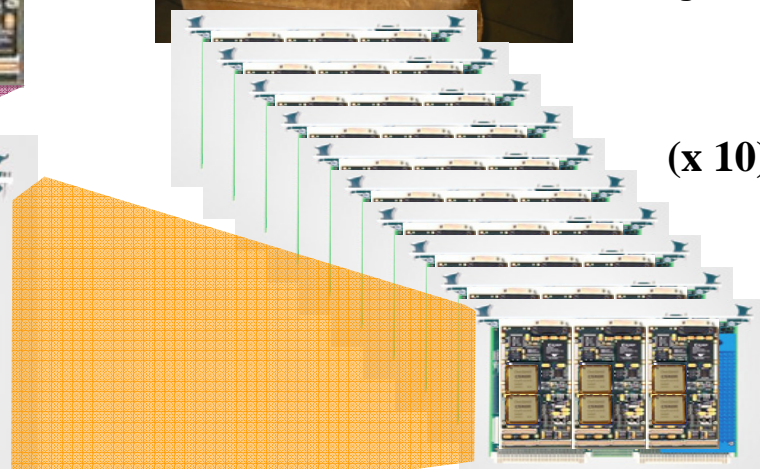
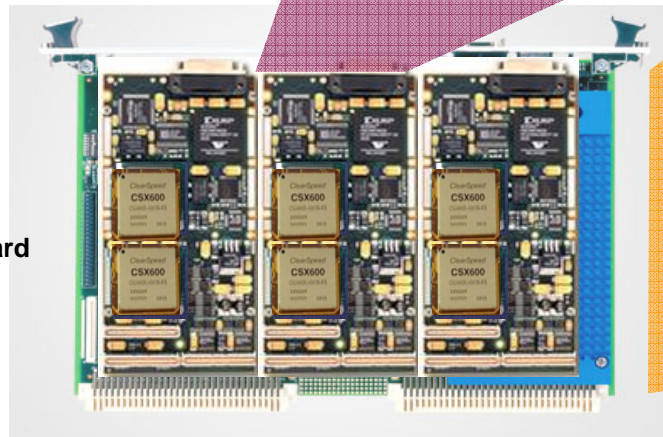


~50 GFLOPS
64-bit FP
SIMD Processor Chip



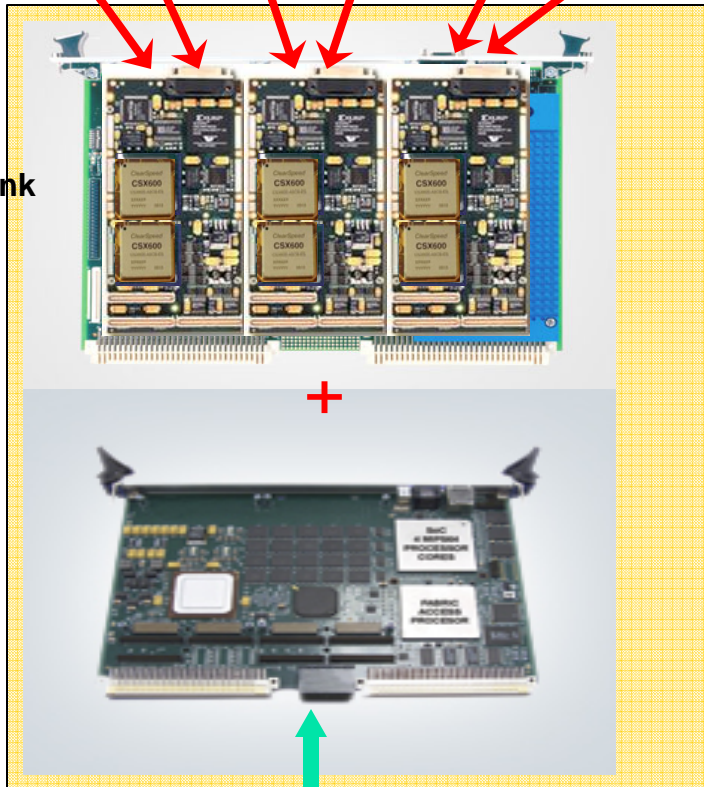
~3 TFLOPS
64-bit FP
Single Rack SPP
(30x – Full Duplex
10 GigEthernet)

~300 GFLOPS
64-bit FP
6U VME Expansion board



(x 10)

CamArray™ Multi-Sensor Platform



6 Cameras
Dual CameraLink
(x3)

6U Host
Motherboard



42 Cameras per Cardcage



With SAN Storage



SAN