Benchmark Results for Ultra-High Performance Scalable Processing Architecture for Embedded Defense Signal and Image Processing Applications

Stewart Reddaway (sfr@wscapeinc.com)¹, Nigel Bond (<u>nigel.bond@wscapeinc.com</u>)¹, Rick Pancoast (rick.pancoast@lmco.com)², Justin Kidman (justin.kidman@wscapeinc.com)¹, (Pete Rogina (pete@wscapeinc.com)¹ World*Scape* Defense Company, LLC¹, 11 Eves Drive, Suite 100, Marlton, NJ 08053, Phone: 856-797-8700, Fax: 856-797-0026 and Lockheed Martin, Maritime Systems and Sensors (MS2)², 199 Borton Landing Road, Moorestown, NJ 08057, Phone 856-722-2354, Fax: 856-722-2055

This briefing provides benchmark results for an ultra-high performance scaled-Single-Instruction/Multiple-Data (SIMD) processing architecture originally designed to realize immersive, photo-realistic 3-D scene capture and playback. This low-power, PMC-based architecture provides for hundreds and ultimately thousands of processing elements, each with optional floating point hardware, to perform data parallel processing on image and signal processing applications as well as for compression, encryption, search, and general sensor processing applications. The technology is supported by a flexible development environment, including assembly language and C-based language support, with plans to develop industry standard API Libraries based upon VSIPL and, ultimately, HPEC-SI. Hardware Pulse Compression Results have been demonstrated at over 100,000 per second per chip when measured DRAM to DRAM and with approximately 95% of cycles being used for filter processing.

The scaled-SIMD technology, named Dupree, is incorporated into PrPMC cards with powerful Processing Elements (PEs), floating-point hardware, and off-board I/O. WorldScape is applying numbers of Dupree boards to radar processing with the current benchmark results demonstrating significantly more performance with much lower power dissipation (GFLOPS/Watt). Implementations with the Dupree hardware provide attractive alternatives to traditional FPGA and DSP solutions. Lockheed Martin is providing testing and support for these implementations. WorldScape has previously demonstrated FFT, Pulse Compression, a form of QR factorization, and other applications on past generations of hardware using a mix of C-level programming and optimized assembly. The current generation CSX600 chip is compatible, but also has several improvements that will significantly enhance I/O performance as well as raw GFLOP throughput. The CSX600 has 48 peak GFLOPS per chip, and the Dupree board has two chips each. Two Dupree cards will be incorporated into a 6U card for scaling.

World*Scape* Defense Company has been developing key algorithms and library functions such as FFTs and FIR filters which efficiently utilize the architecture and floating point per PE hardware to gain exceptional performance at very low power dissipation levels. Specific application work, supported by the Office of Naval Research, has been undertaken for radar processing with raw throughput numbers for functions such as FFTs, complex multiplies, filters, etc. significantly higher than other industry standard processing and DSP platforms. This briefing also describes new levels of benchmark performance for FFT per second per watt that provide the basis of plans for embedded SAR processing systems on small UAV's using WorldScape's Scalable Processing Platform (SPP). High level C and VSIPL library support are planned and currently under development.

Lockheed Martin Maritime Systems and Sensors (MS2) has been trained in the use of the SIMD SDK, and has ported some key, high-performance application benchmarks for performance comparison with general purpose processing architectures. Results have shown the potential for considerable performance enhancement for airborne, shipboard, ground-based and undersea tactical signal and image processing systems. Lockheed Martin has also supported WorldScape in the SPP architecture design as an industry partner.

In this briefing, WorldScape and Lockheed Martin will present updated hardware benchmark demonstrations and discuss a Scalable Processing Platform for embedded radar processing which significantly improves I/O performance and provides a roadmap to government-qualified hardware for technology insertion. Architectures, data parallel coding approaches, additional functionality of the Scalable Processing Platform, and relevance to embedded defense radar applications will be discussed. Finally, the results of a DoD benchmark algorithm run on the COTS SIMD CSX600 will be presented and compared with general purpose processor performance.