DFT Compiler for FPGA and CPU/FPGA Partitioned Implementations

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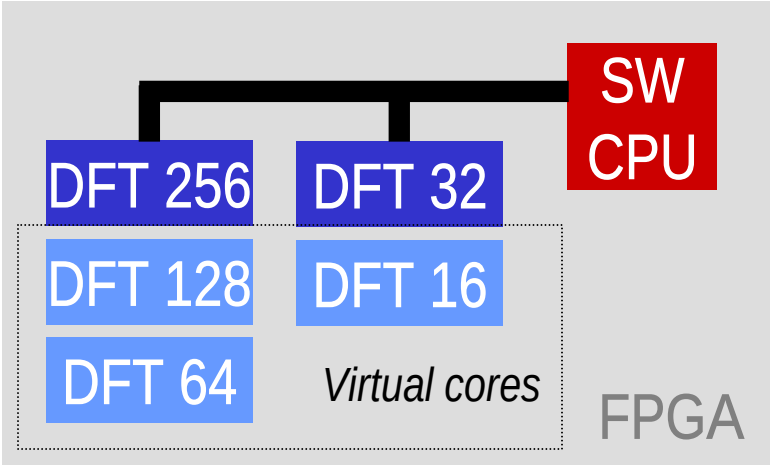
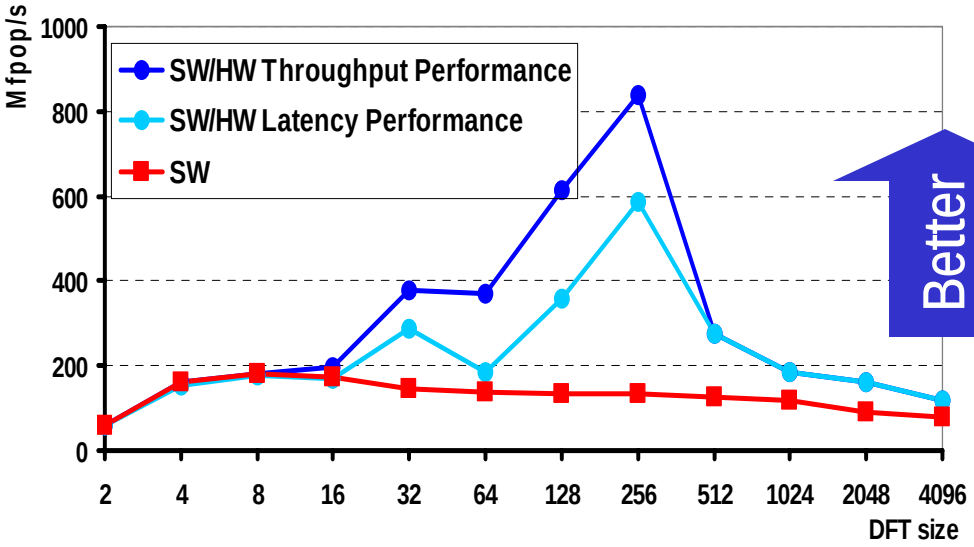
DFT Compiler for CPU/FPGA: From Math to Code

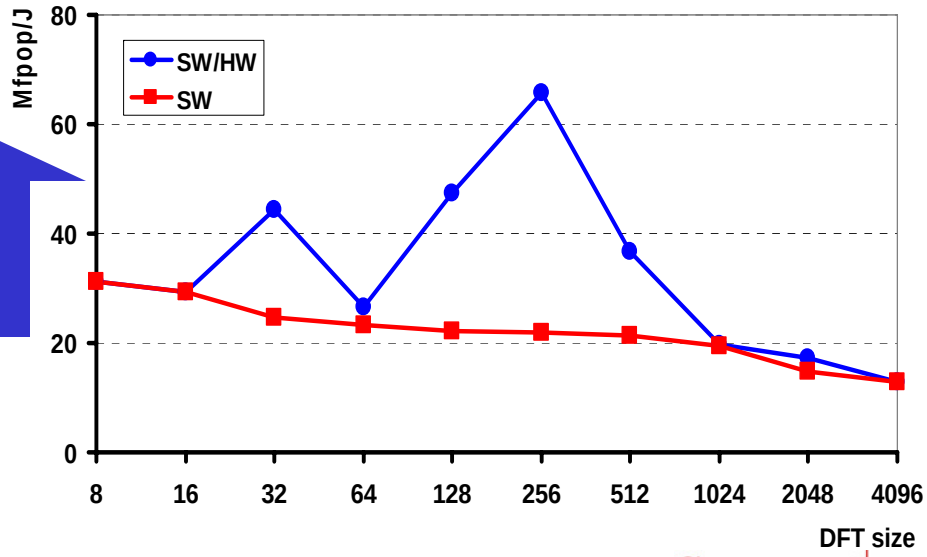
- Choose two HW IPs: HW DFT(32) and DFT(256)
- Connect the HW DFTs and CPU by OCM bus
- Generate an HW-SW interface for the system
  - Core Virtualization (DFT 16, 64,128)
- Generate a library for any DFT(2^n) using Spiral



Speedup over SW



Energy Efficiency over SW



Formula-Driven Synthesis: From Math to RTL Verilog

$$\mathrm{DFT}_{1024}$$

transform

$$\left[\prod_{k=0}^{4} L_4^{4^5}\,(I_{4^4}\otimes \mathrm{DFT}_4)\,D_k^{4^5}\right] R_4^{4^5}$$

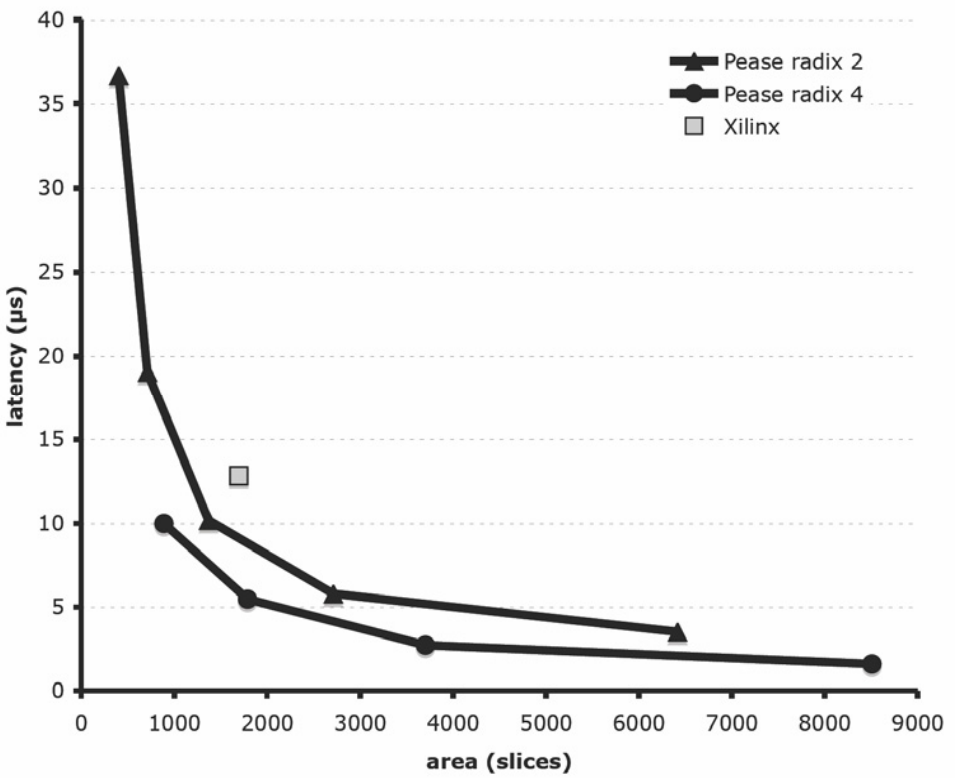
formula

$$\underbrace{\left[\prod_{k=0}^{4}{}^{\mathrm{ir}}\, L_4^{4^5}\,(I_{4^4}\otimes \mathrm{DFT}_4)\,D_k^{4^5}\right] R_4^{4^5}}_{\mathrm{stream}(8)}$$

hardware parameters

$$\left[\prod_{k=0}^{4}{}^{\mathrm{ir}}\, \underbrace{L_4^{4^5}}_{\mathrm{stream}(8)}\,(I_{128}\otimes^{\mathrm{sr}}(I_2\otimes \mathrm{DFT}_4))\,\underbrace{D_k^{4^5}}_{\mathrm{stream}(8)}\right] \underbrace{R_4^{4^5}}_{\mathrm{stream}(8)}$$

hardware formula



$$\mathrm{DFT}_{1024}$$