

RFIC Beamforming for Agile, Low-Cost Overlapped Subarrays

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Abstract

An overlapped subarray architecture using RFIC beamforming represents an approach for implementing multiple digital beams in a cost effective manner. The RFIC beamformer uses an RF-CMOS process to provide analog pre-processing of the received signal with controllable weights prior to subarray digitization. A preliminary RFIC beamformer chip design demonstrates the technique, with measured and calculated data showing close agreement. A second chip design was implemented with an on-chip X-band low-noise amplifier. This design is packaged and mounted on an integrated overlapped subarray for near- and far-field pattern testing.

Introduction

Electronically scanned arrays require a minimum number of controls, N_{\min} , given by the number of orthogonal beams that fill a prescribed scan sector [1]. Most practical antenna arrays require considerably more than N_{\min} control elements, but overlapped subarray architectures can approach this theoretical limit. Figure 1 shows a block diagram of an overlapped subarray architecture. The overlapped subarray network produces a flat-topped sector pattern with low sidelobes that suppress grating lobes outside of the main beam of the subarray pattern. Each radiating element of the array is connected to multiple subarrays, creating an overlapping geometry. It is possible to scan one beam, or a fixed set of contiguous beams, over the main sector of the subarray with a set of N_{\min} phase shifters. Alternatively, digital receivers can be connected to the N_{\min} subarrays and multiple simultaneous beams can be formed digitally. Digital subarray architectures using a combination of element level phase shifters and subarray level receivers makes it possible to scan multiple beam clusters over all space.

A conventional approach to the design and manufacturing of the overlapped subarray network shown in Figure 1 is challenging and costly due to the complexity of the microwave network [2]. However, the design of the overlapped subarray beamformer using Radio Frequency Integrated Circuits (RFIC) represents a novel approach for implementing an efficient trade-off between the agility and capability of fully digital arrays and the cost effectiveness of analog arrays.

Approach

The realization of a practical overlapped subarray antenna for a radar system presents many challenges [2]. The overlapped subarray network implemented in a standard multilayer printed circuit board requires many layers leading to a large and expensive RF front-end as shown in Figure 2. In this work, the weighting and summing functions of the overlapped subarray network shown in Figure 1 are performed in an RFIC using an RF-CMOS process leading to a significant reduction in board complexity and cost. Additionally, some of the inevitable errors in the analog front-end can be compensated by tuning the weighting functions, allowing more tolerance in the design and manufacturing of the RF front-end.

The use of an RFIC beamformer has an additional advantage that the weights shown in Figure 1 are adjustable and controllable. However, to minimize IC size and DC power consumption, the weights are implemented with amplitude control only with a 180° phase difference possible. These weights can be adjusted to implement a flat topped sector beam [2] or other possible subarray patterns. The RFIC beamforming approach to the electronically scanned array provides some pre-processing of the received pattern before reaching the analog-to-digital converter. This is important in a phased array environment, particularly for X-band frequencies and higher, where minimizing the complexity of the hardware leads to lower cost.

Results

An initial RFIC design using a $0.18 \mu\text{m}$ RF-CMOS process has been fabricated and tested to prove the concept of constructing arrays in this manner. Measured and simulated data of the RFIC design in Figure 3 show close agreement. Using a fully differential topology, an input buffer is placed at each of the four inputs. The input buffer can be a low noise amplifier or vector modulator for a fully integrated RF front-end receiver. The amplitude weighting is accomplished by variable gain amplifiers implemented using a Gilbert cell architecture operating in a linear mode [3]. The Gilbert cell architecture provides continuous amplitude control while also a means for changing the output phase by 180° . The four weights are summed at the final stage output buffer amplifier and matched on the output to 50Ω . The differential input match (S_{11}) is designed and measured for -10dB at 10 GHz as demonstrated in Figure 3b. The insertion loss (S_{21}) from

input 1 to output 2 is shown in Figure 3b. Little effort was made in this initial RFIC design to flatten the gain across the band of interest 9-11 GHz. The measured DC power consumption was 284 mW.

A second design using a 0.13 μm RF-CMOS process with an integrated low-noise amplifier has higher simulated gain (12dB), lower noise figure (3.6 dB) and less power (200 mW) and was implemented for use in an X-band overlapped subarray demonstration. The second RFIC is integrated in a standard quad flat pack no-lead (QFN) package and mounted on an array for near- and far-field pattern testing. Results will be shown in the presentation.

References

- [1] R. Mailloux, *Phased Array Antenna Handbook*, Artech House, Boston, MA (1993).
- [2] J.S. Herd, S.M. Duffy, and H. Steyskal, "Design considerations and results for an overlapped subarray radar antenna," *IEEE Aerospace Conf. Dig.*, Big Sky, MT (2005).
- [3] T.H. Lee, *The Design of CMOS Radio-Frequency Integrated Circuits* 2nd edition, Cambridge University Press, 2004.

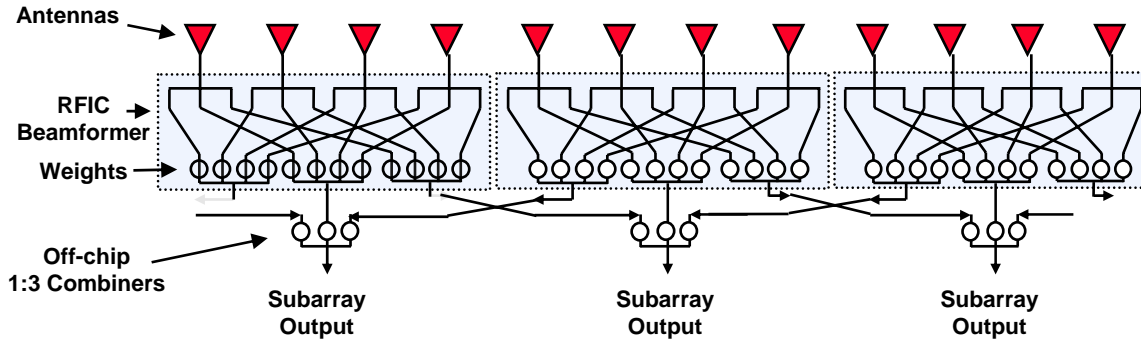


Figure 1 – 12-element overlapped subarray block diagram.

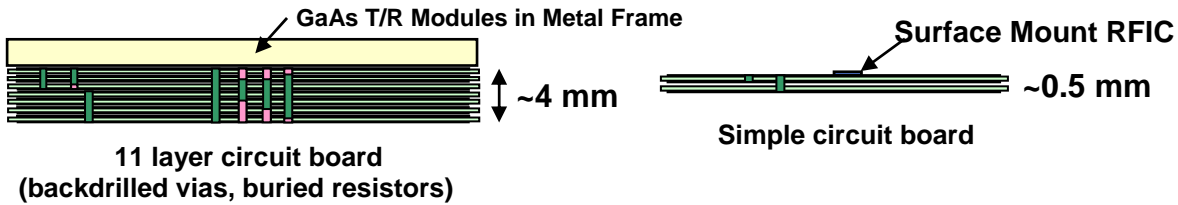


Figure 2 – Conventional multilayer printed circuit board beamformer vs. RFIC beamformer.

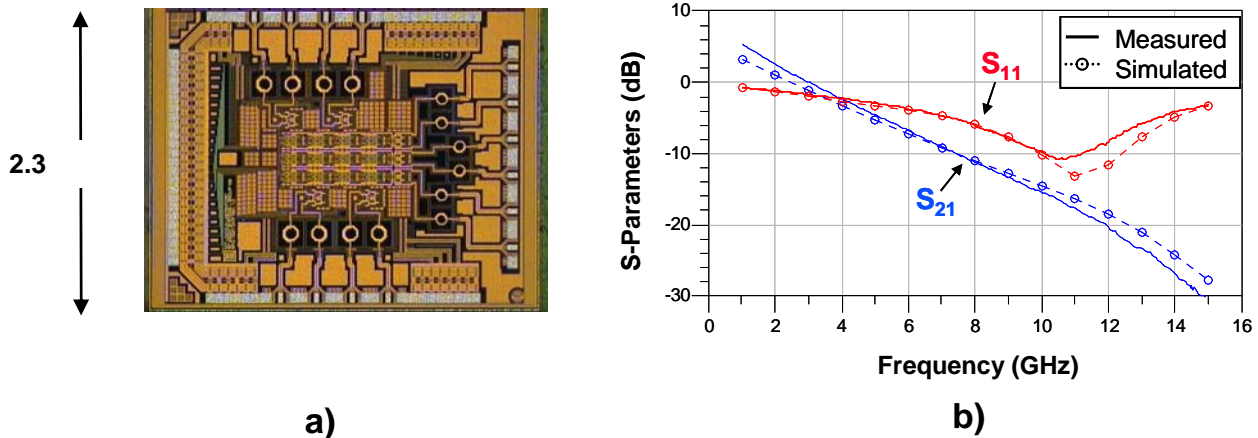


Figure 3 – Proof-of-concept RFIC beamformer design. a) die picture, b) measured and simulated results.