


MONARCH: A First Generation Polymorphic Computing Processor

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IBM

Computer Systems, Inc. MERCURY

SE

CREST at GEORGIA TECH

Exogi

USC SCHOOL ENGINEER

ISI Information Sciences Institute

Outline

- Application needs that drive MONARCH like processors
- MONARCH summary
- Architecture details
- Processor chip description
- Transitions and summary

Embedded Processing Architectures Ten Year Vision (2004-2014)

Market/Technology Trend

Mission Changes

- Need for waveform diversity and interference rejection
- Growing number of sensor channels at GHz conversion rates
- Growing use of adaptive algorithms
- Higher resolution sensors
- More use of autonomous, small sensors and battery powered ground sensors
- More demand for space based sensors
- Desire/need for direct transmission of info to users
- Commercial trends drive Semiconductors
  - Cellular market processors
  - Game market
  - Reprogrammable FPGAs

Impact

System Implications

- Digital interface is moving forward using higher speed A/Ds
- Higher speed I/O (10-50 GB/S)
- Higher throughputs (.1-100 TOPS)
- Growing need for power efficient processing
- Larger memory storage (->1TByte)
- Space assets become integral part of terrestrial fire control
  - Higher on-orbit throughputs
- Communication of information between all assets, in dynamically changing network is essential
  - Plug and play critical
- More embedded intelligence within sensors and weapons
- Power/heat impact on electronics

From space to ground, multiple applications need efficient processing

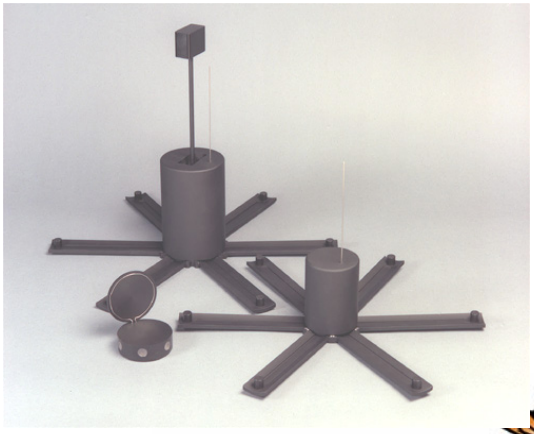
TOPS – Tera Operations Per Second
STAP – Space Time Adaptive Processing
IRST – InfraRed Search and Track
HSI – Hyper Spectral Imaging
ATR – Automatic Target Recognition

Space Sensors

- On Orbit 1-5 TOPs throughput - programmable
- STAP RADAR processing
- HSI processing
- Image formation

Unattended sensors

- 1 GOPS on batteries
- Digital receivers
- ATR
- Multi sensor fusion



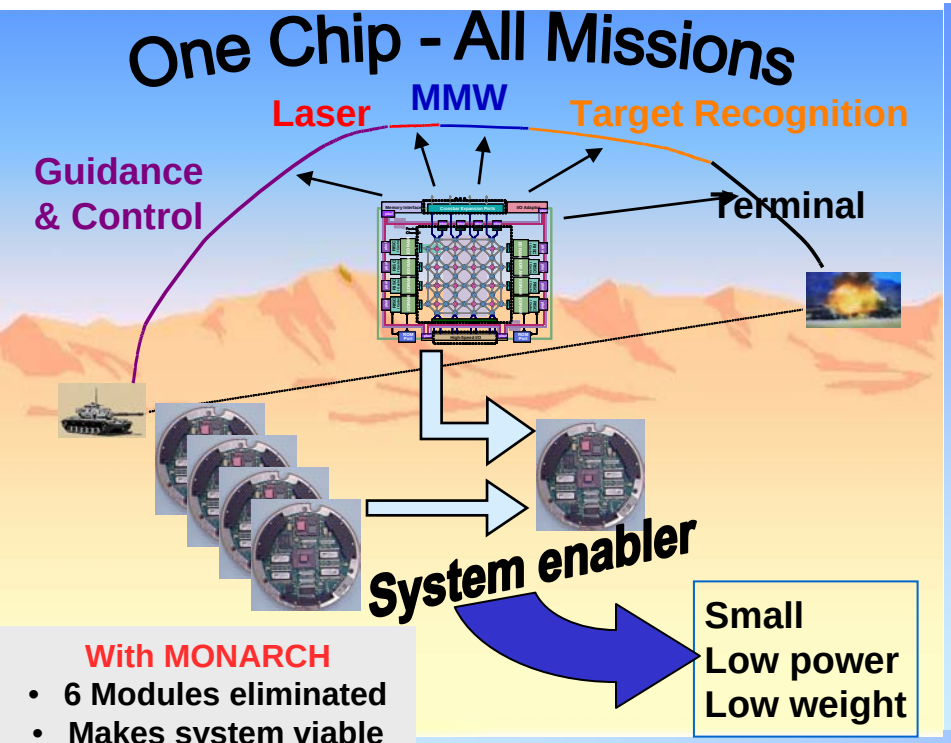
Airborne Multi-sensor Processing

- 3-5 TFLOPS in one chassis
- STAP processing (150 channels)
- IRST
- Multi sensor fusion

MONARCH

MONARCH Morphs to Mission Needs

One Chip - All Missions



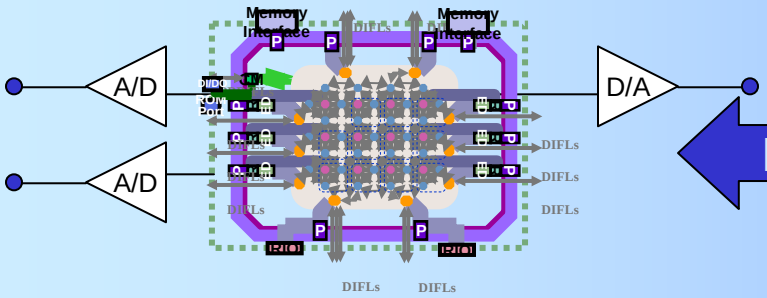
With MONARCH
- 6 Modules eliminated
- Makes system viable



Ground Air Space

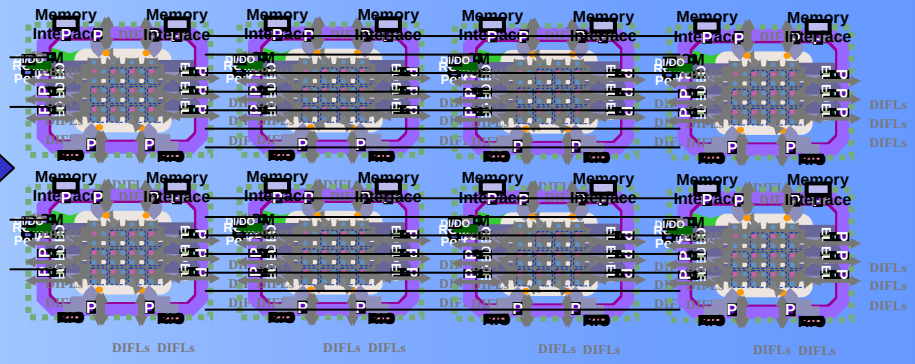
- **Multi Function on single chip**
  - ***Radar, EO*, HSI, *Com*, SIGINT**
- **Replace many ASIC types with 1 chip**
- **Energy efficient architecture**
  - **Reconfigurable logic**
  - **Multiple GFLOPS/Watt**
  - **Self contained controllers**
    - **6 RISC processors + 12 MB RAM**
  - **>40 GBytes/S I/O with built in switch**

System on a Chip – Deeply embedded



BOTH

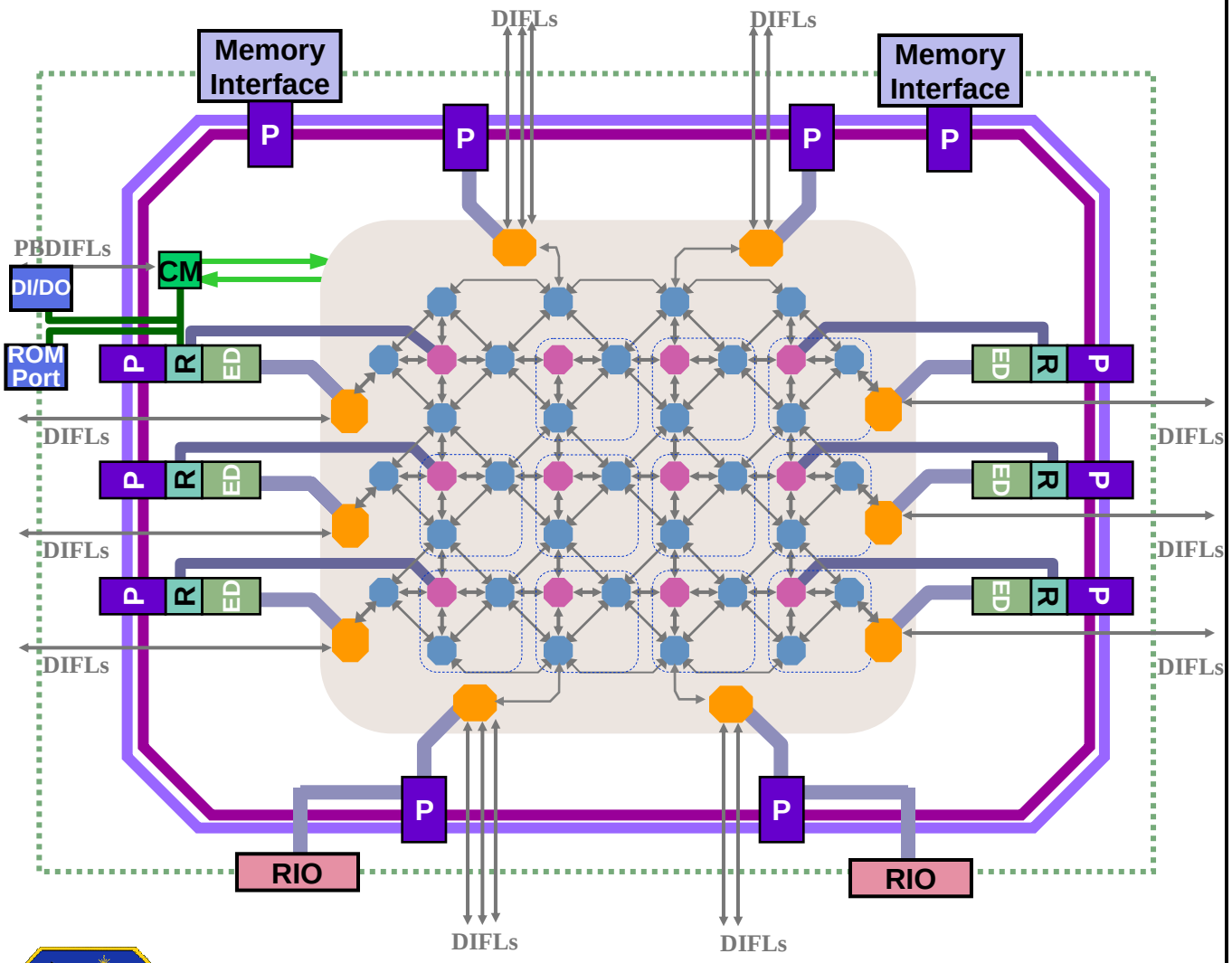
Replicated chip – Embedded TeraFLOPS



MONARCH = MOrphable Networked micro-ARCHitecture

MONARCH Chip Architecture

Rev 12-Mar-06

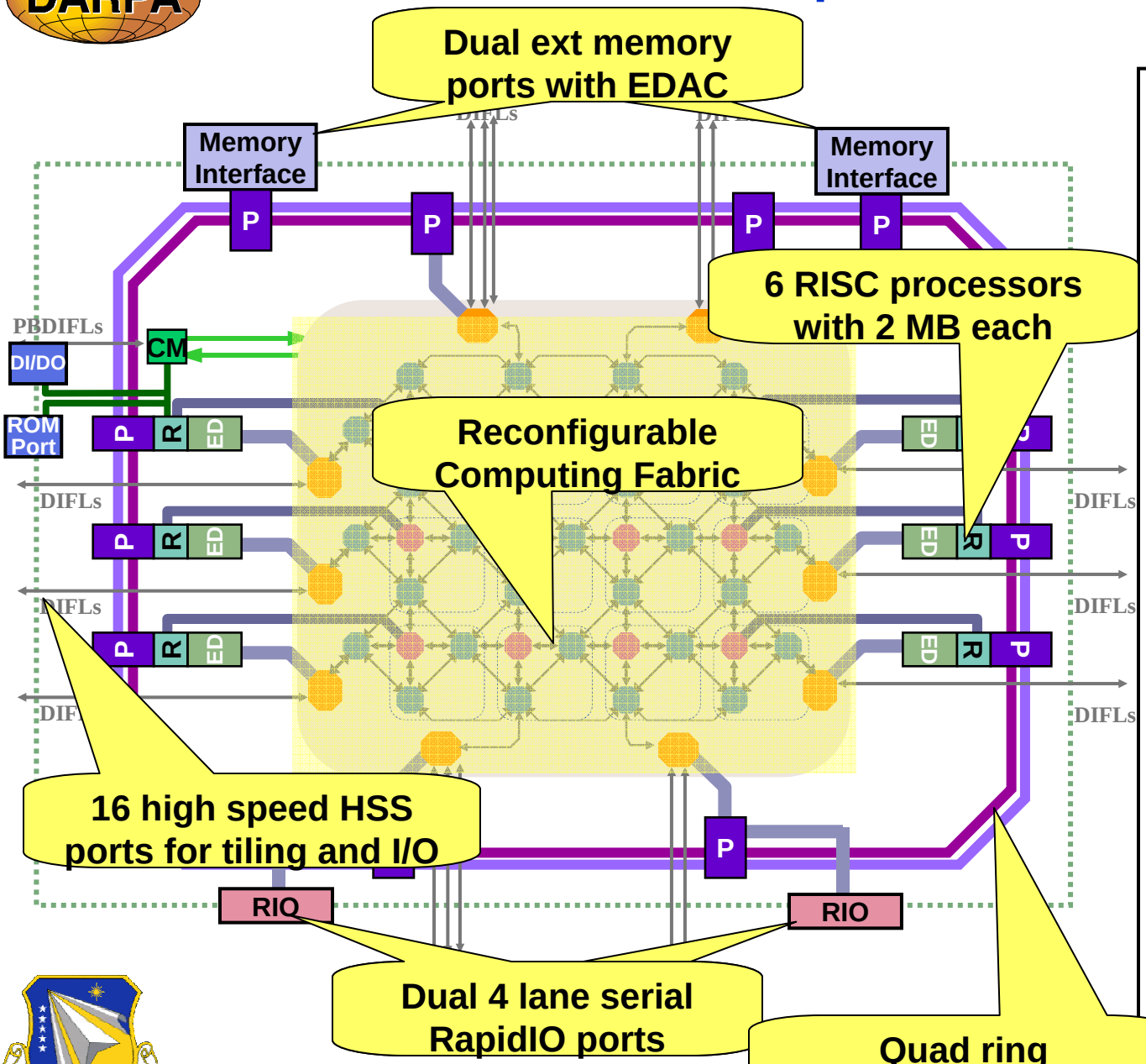


- **Throughput 64 GOPS peak**
- **Multiple programming modes**
  - Reconfigurable, data flow
  - RISC scalar
  - RISC SIMD (Altivec-like)
- **90 nm bulk CMOS**
- **Clock 333 MHz**
- **Power 3-6 GFLOPS/W**
- **12 Arithmetic Clusters**
  - 96 adders (32 bits) fixed and float
  - 96 multipliers
- **31 Memory Clusters**
  - 124 dual port memories
  - 256W x 32 bits each (128KB)
  - 248 address generators
- **>72 DMA engines**
- **6 RISC processors**
- **12 MBytes on chip DRAM**
- **2 Bulk memory interfaces (8 GB/s BW)**
- **2 RapidIO (serial) interface**
- **17 DIFL ports (2.6 GB/s ea)**
- **On-chip ring 40 GB/s**

DIFL =Differential Inter FPCA Link

MONARCH

MONARCH Chip Architecture



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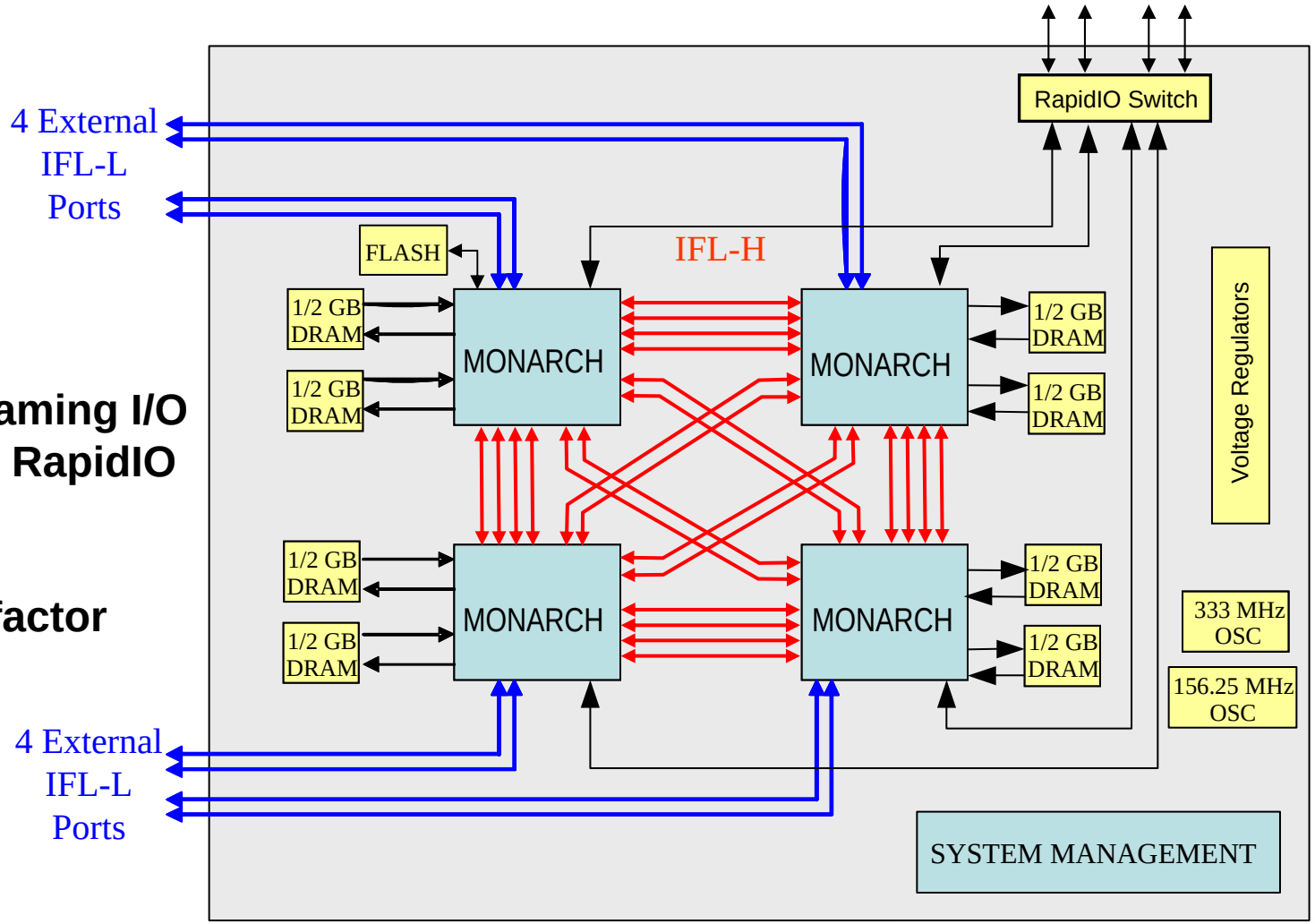
MONARCH

QUAD MONARCH Module

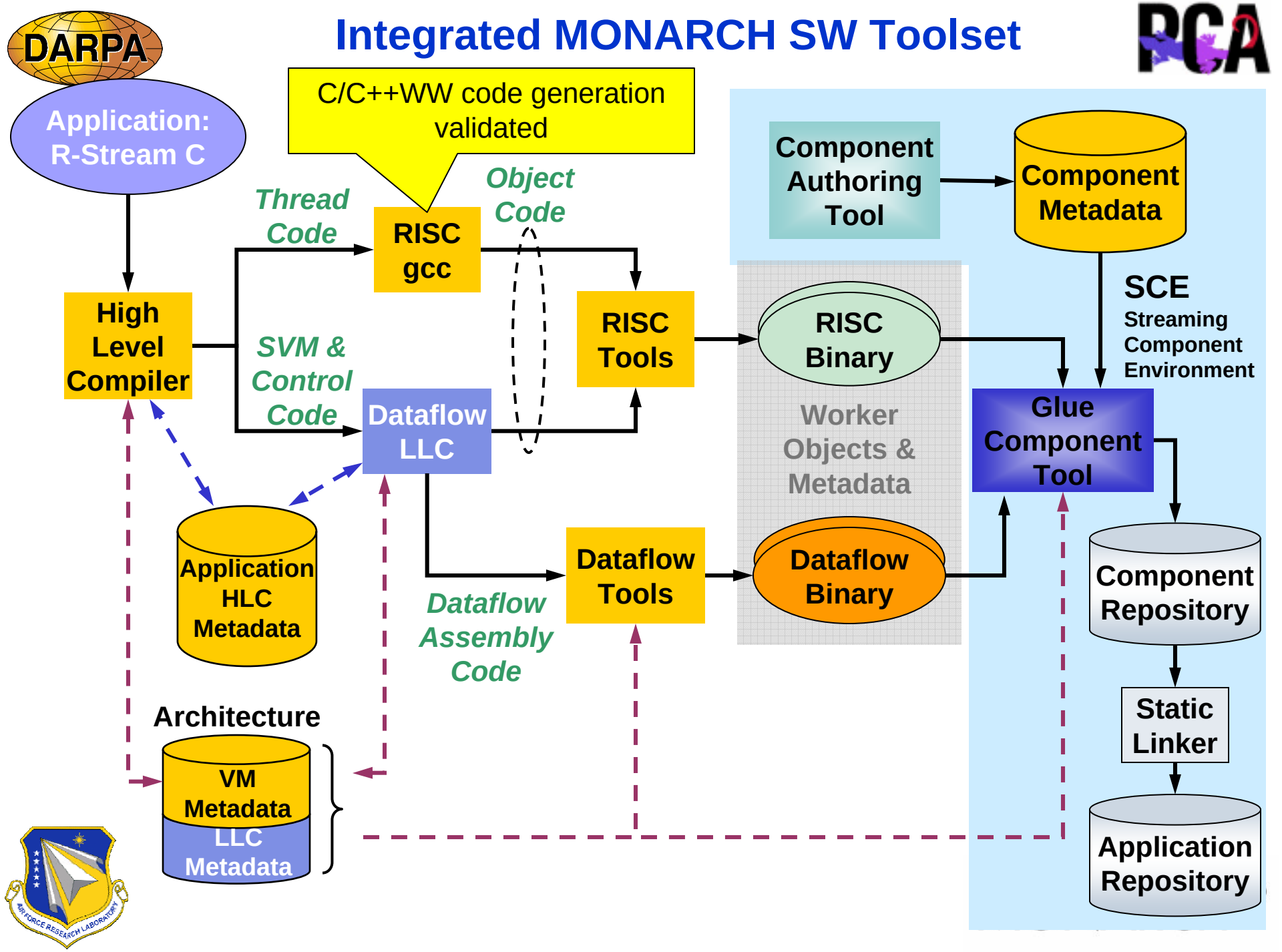
High speed network connection built into MONARCH chips
Standard connectors and interfaces – compatible with MC product line
No support chips required – built in memory and high speed I/O interfaces

256 GFLOPS
4 GBytes RAM
32 MBytes Flash
8 High speed streaming I/O
4 quad lane Serial RapidIO
JTAG/SM
- **6U-160 feasible**
- **Vita 41/48 form factor**



MONARCH

Integrated MONARCH SW Toolset



Architecture Description

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Native Computing Modes

- **Threaded mode – instruction stream operation**
  - RISC processor with extensions
  - WideWord developed through morphing

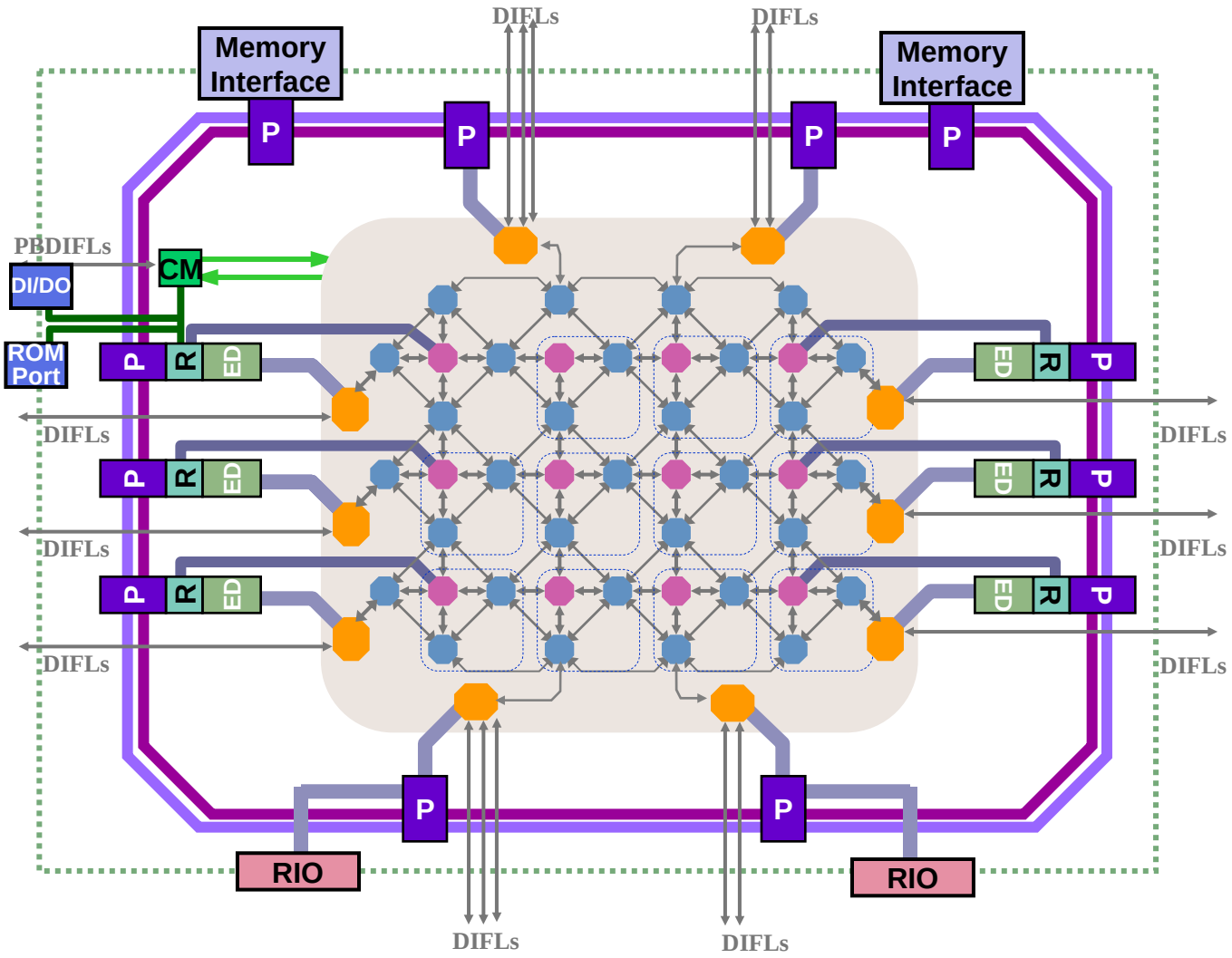
  Use this mode for complex code sets

- **Streaming mode – data flow stream operation**
  - Field Programmable Computing Array

  Use this mode for high data rate and highest throughput

- **Morphing support**
  - FPCA configurable at very fine level
    - Data movement – rich crossbar interconnections
    - Processing elements – ALUs and registers
  - RISC WideWord

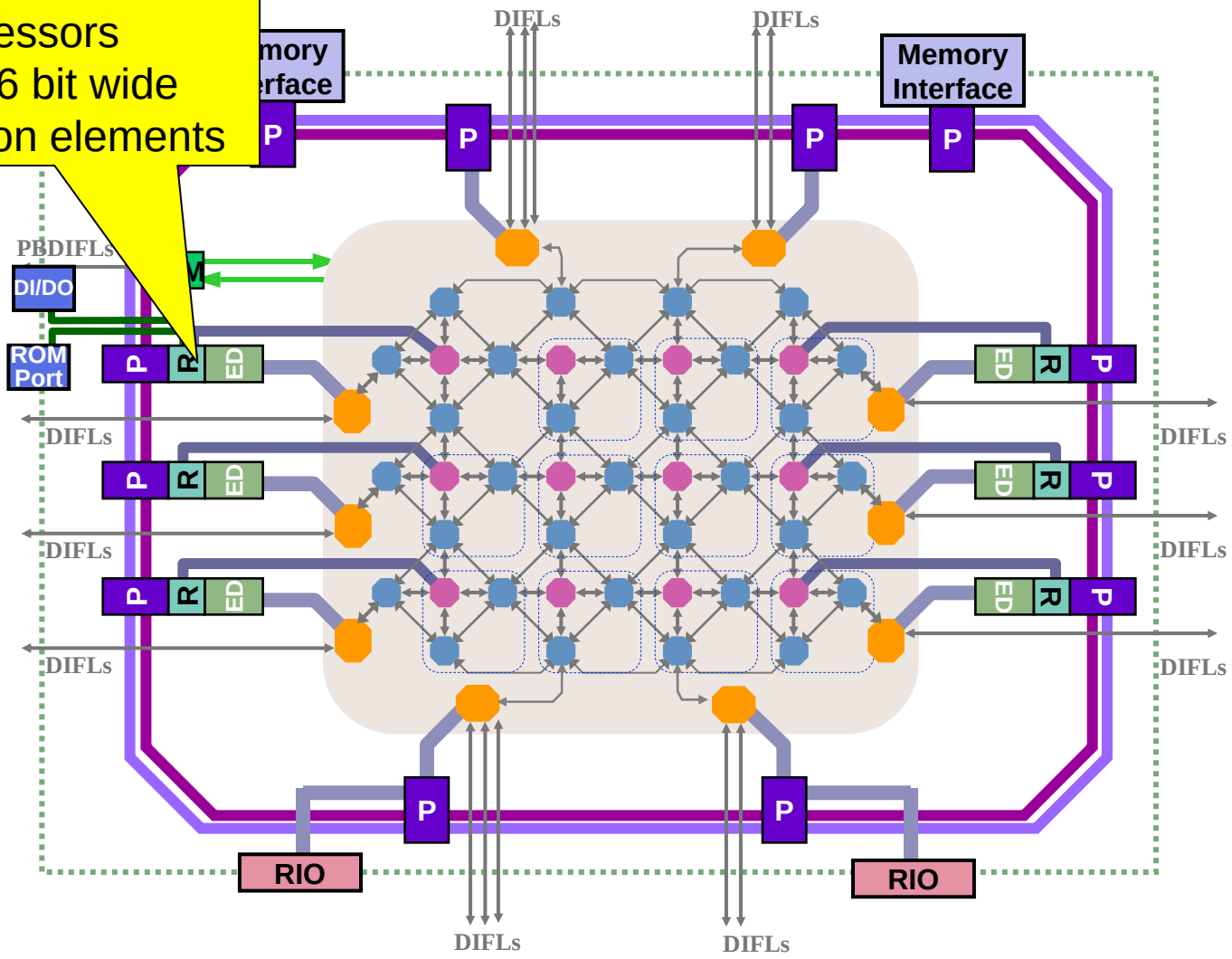
MONARCH Multiple Computing Modes



DIFL =Differential Inter FPCA Link

MONARCH Multiple Computing Modes

Mode 1:
6 conventional RISC processors
With 256 bit wide computation elements



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Mode 1:
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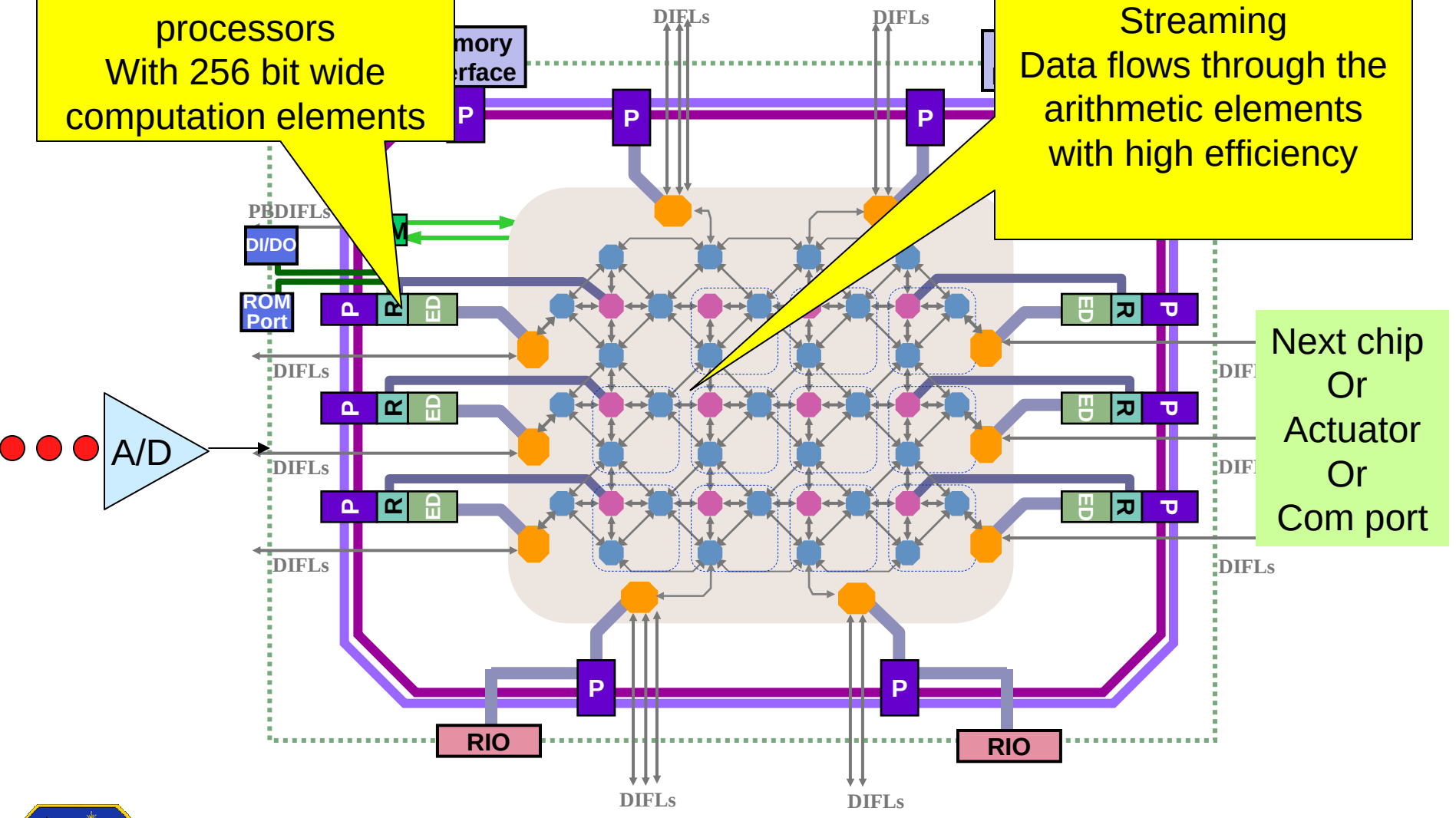
Mode 2:
Streaming
Data flows through the arithmetic elements with high efficiency



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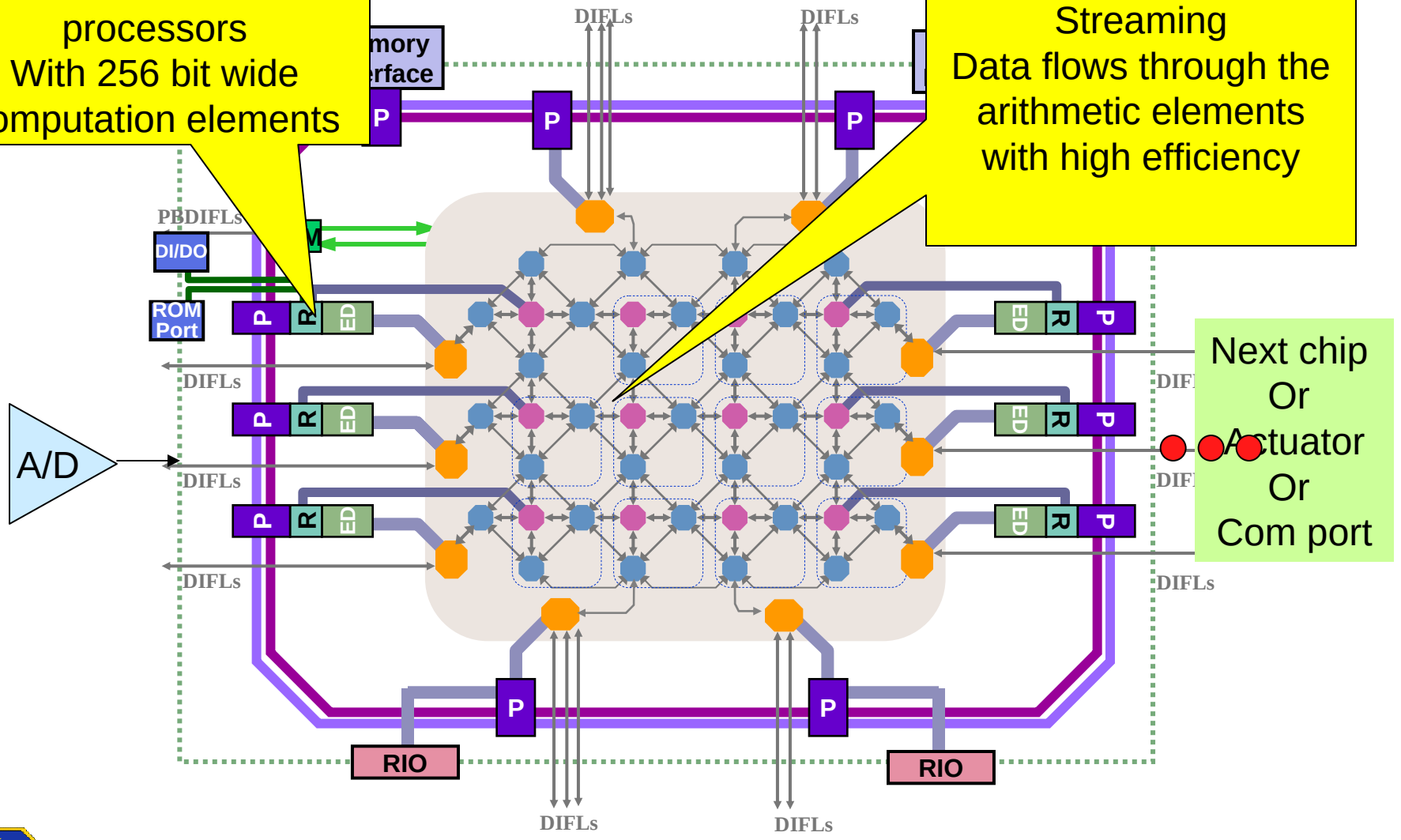

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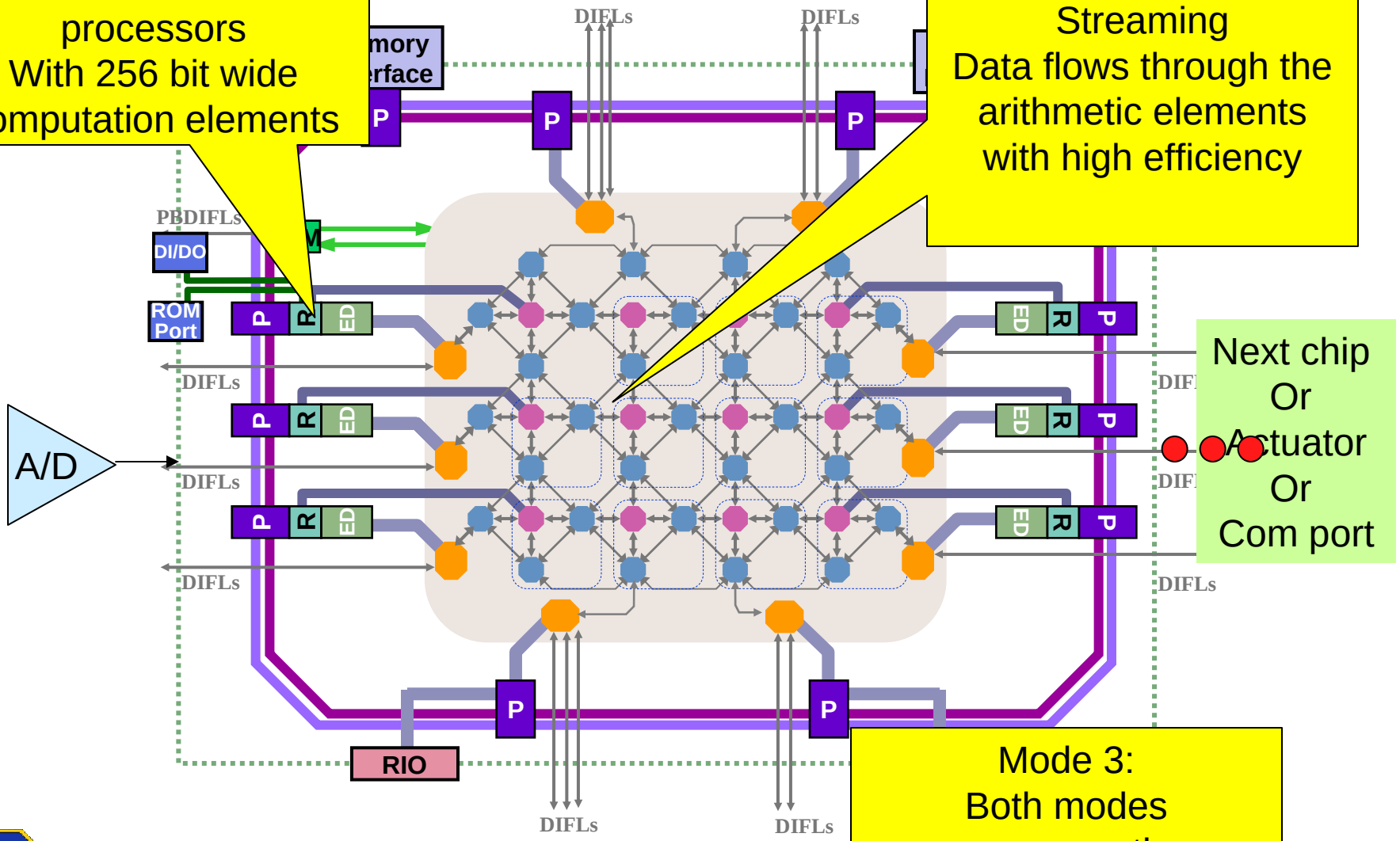
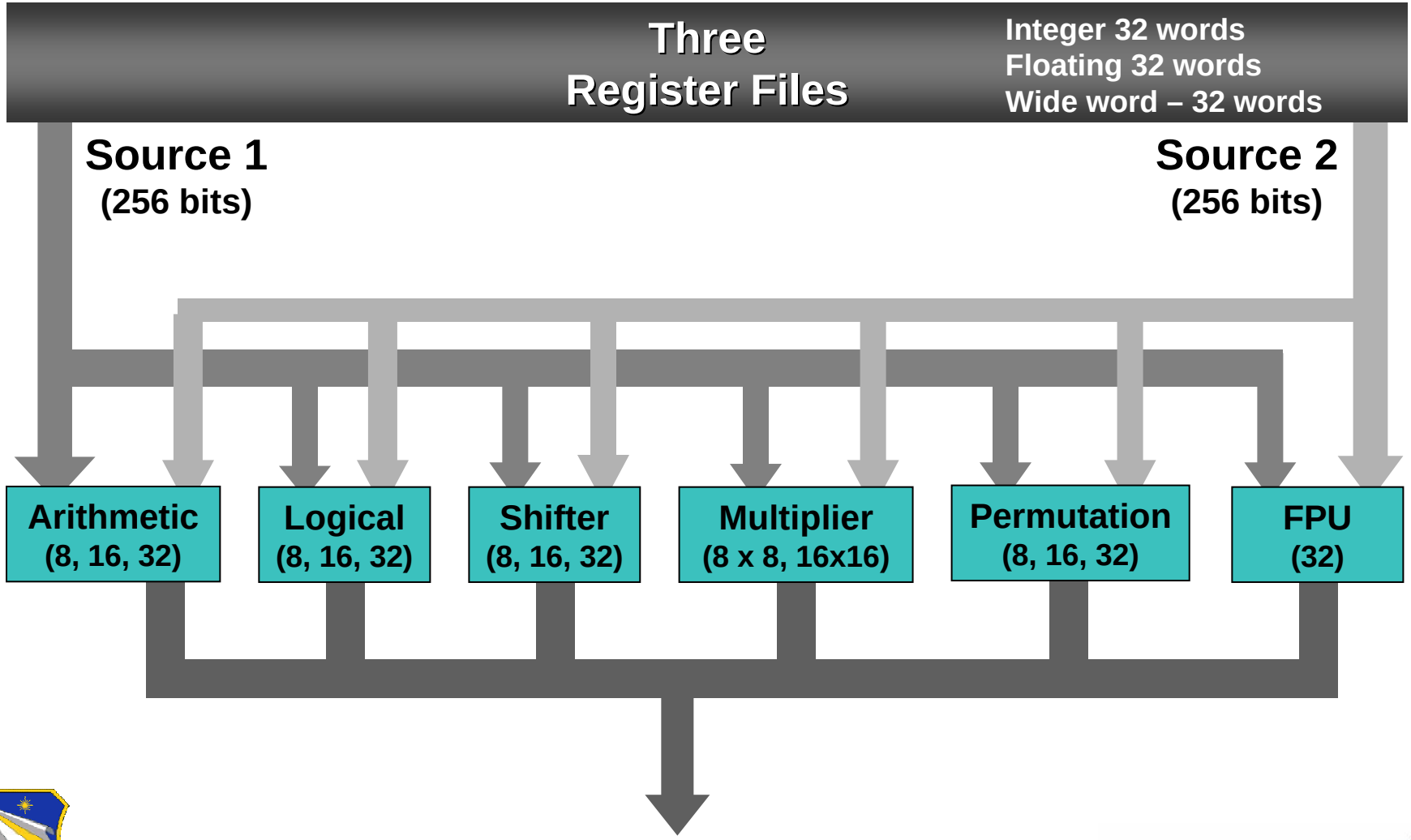


Mode 3:
Both modes concurrently

DIFL =Differential Inter FPCA Link

Threaded Processing

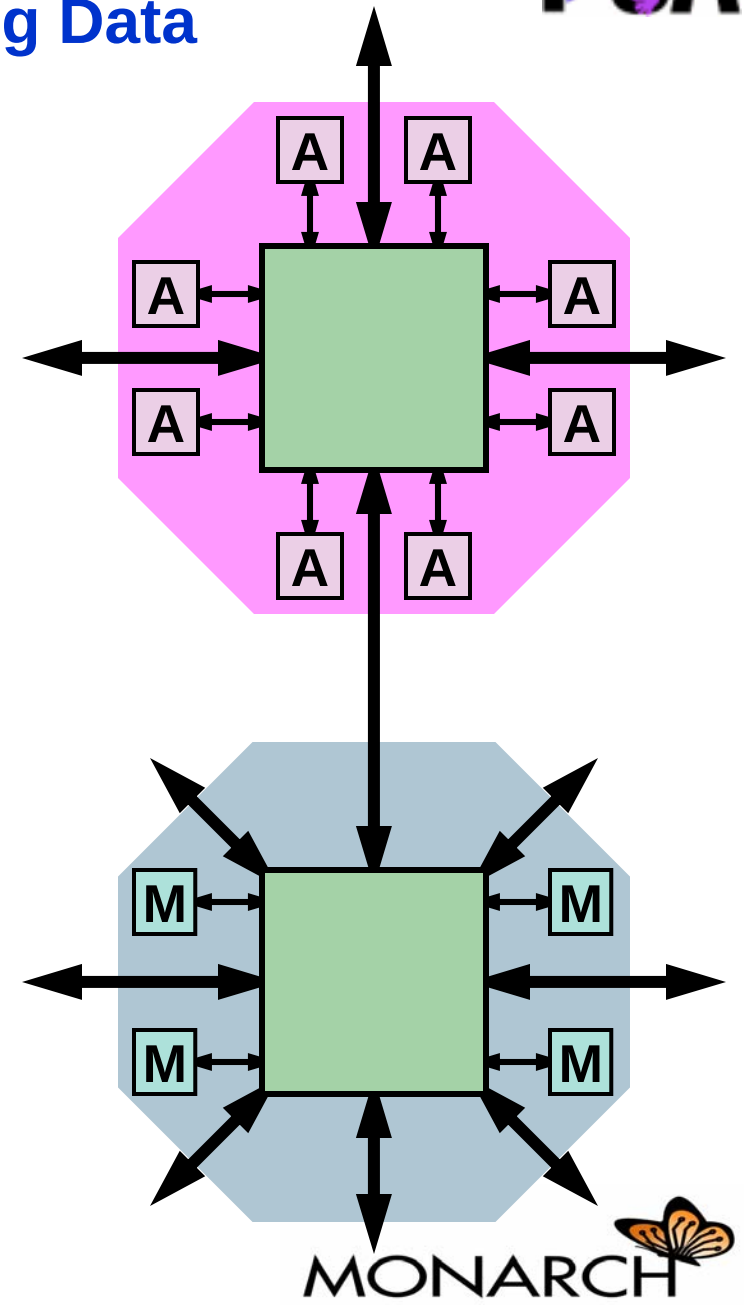
Scalar RISC plus 256 bit wide word
8, 16, or 32 bit data
Intermixed scalar and wide word instructions



FPCA Clusters For Streaming Data

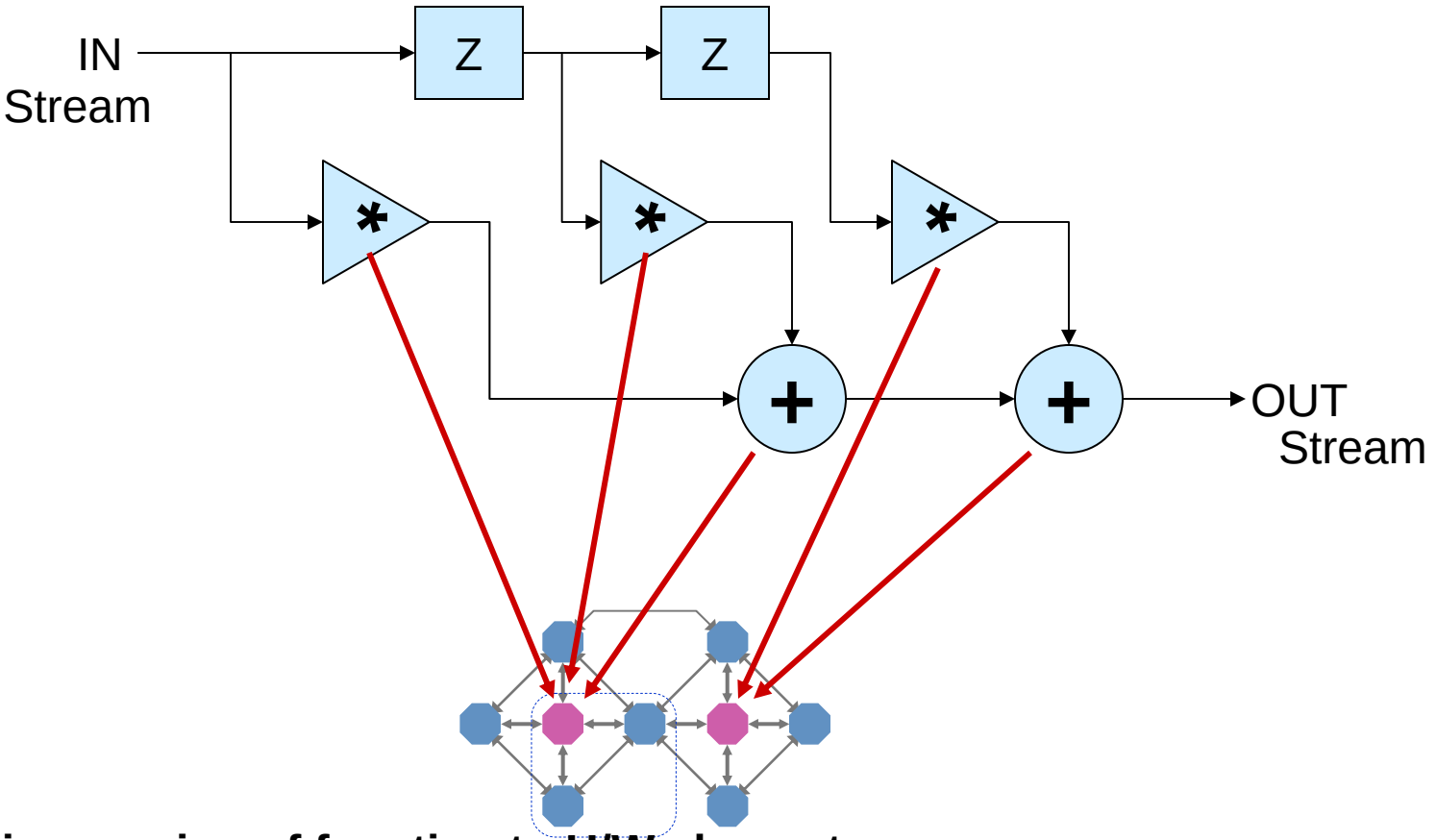
- FPCA Arithmetic Cluster
  - **Eight floating-point MALUs**
    - **32b integer and floating point**
    - **Arithmetic/logical shifter**
  - **Core interconnect fabric**
    - **Multiple links to 4 nearest neighbors**

- FPCA Memory Cluster
  - **4 dual-port memories**
    - **256w x 32b**
    - **Memories can be concatenated**
    - **Individual R/W address generators**
  - **Simultaneous read/write**
  - **Core interconnect fabric**
    - **Multiple links to 8 nearest neighbors**



MONARCH

Streaming FPCA – Basic Paradigm



- Static mapping of function to H/W element
- Self synchronized dataflow (element "computes" when data available)
- Distributed control system for dynamic/data dependent operations
  - 32 bit data + 2 bits of token for control/status/condition code
  - Programmable Logic Array (PLA) in each element for control

Where MONARCH is Most Applicable

Embedded applications with 0.1->10 TFLOP throughput

High data rate – Streaming

Direct processing of multi GigaByte per second input streams

Power, volume, weight constrained applications

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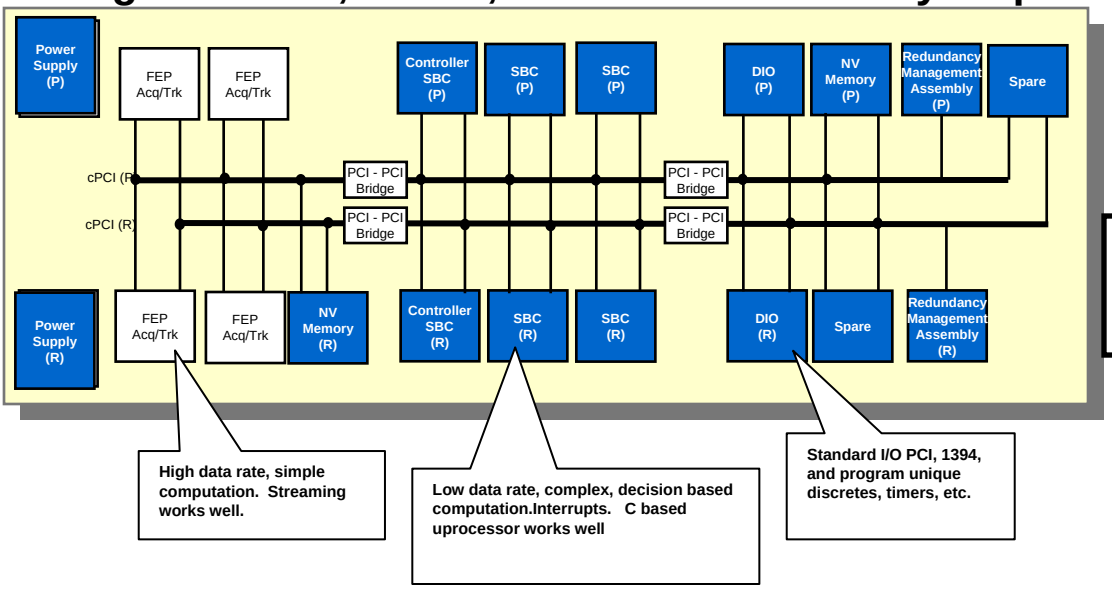
Example of MONARCH benefits for Representative Space EO System

Using PowerPC, ASICs, and discrete memory chips



High data rate, simple computation. Streaming works well.

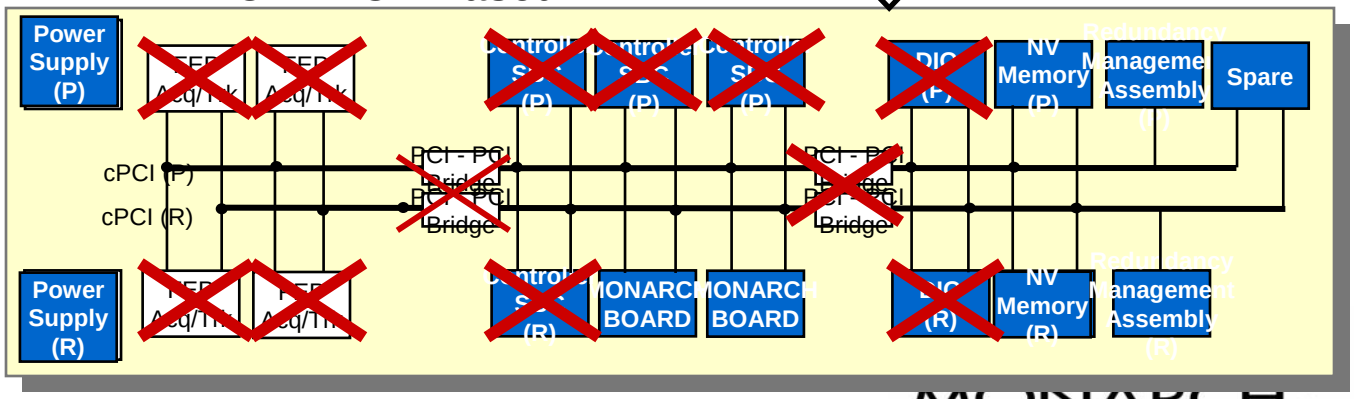
Low data rate, complex, decision based computation.Interrupts. C based uprocessor works well

Standard I/O PCI, 1394, and program unique discretes, timers, etc.

With MONARCH

- 16 modules reduces to 6
- Power drops from 200+ watts to 40 watts
- 5 Fewer chip types

MONARCH Based



MONARCH

UAV RADAR/EO Signal Processor

3 for control
7 for EO/IR compression
6 for others

4 for control
6 for mosaic
6 for auto-focus

48 for signal processing

Each square represents G4 processor

9 U Processor Boards

P++ Raceway (66 MHz)

P++ Raceway (66 MHz)

DataRate = 2x256MB/s

With MONARCH

Five boards becomes less than one board – Programmability retained!

Less weight, power, cost

Greater endurance or more functions

0.5 for control
1 for EO/IR compression
1 for others

0.5 for control
1 for mosaic
0.1 for auto-focus

2.9 for signal processing

Monarch High Speed I/O (1 GHz)

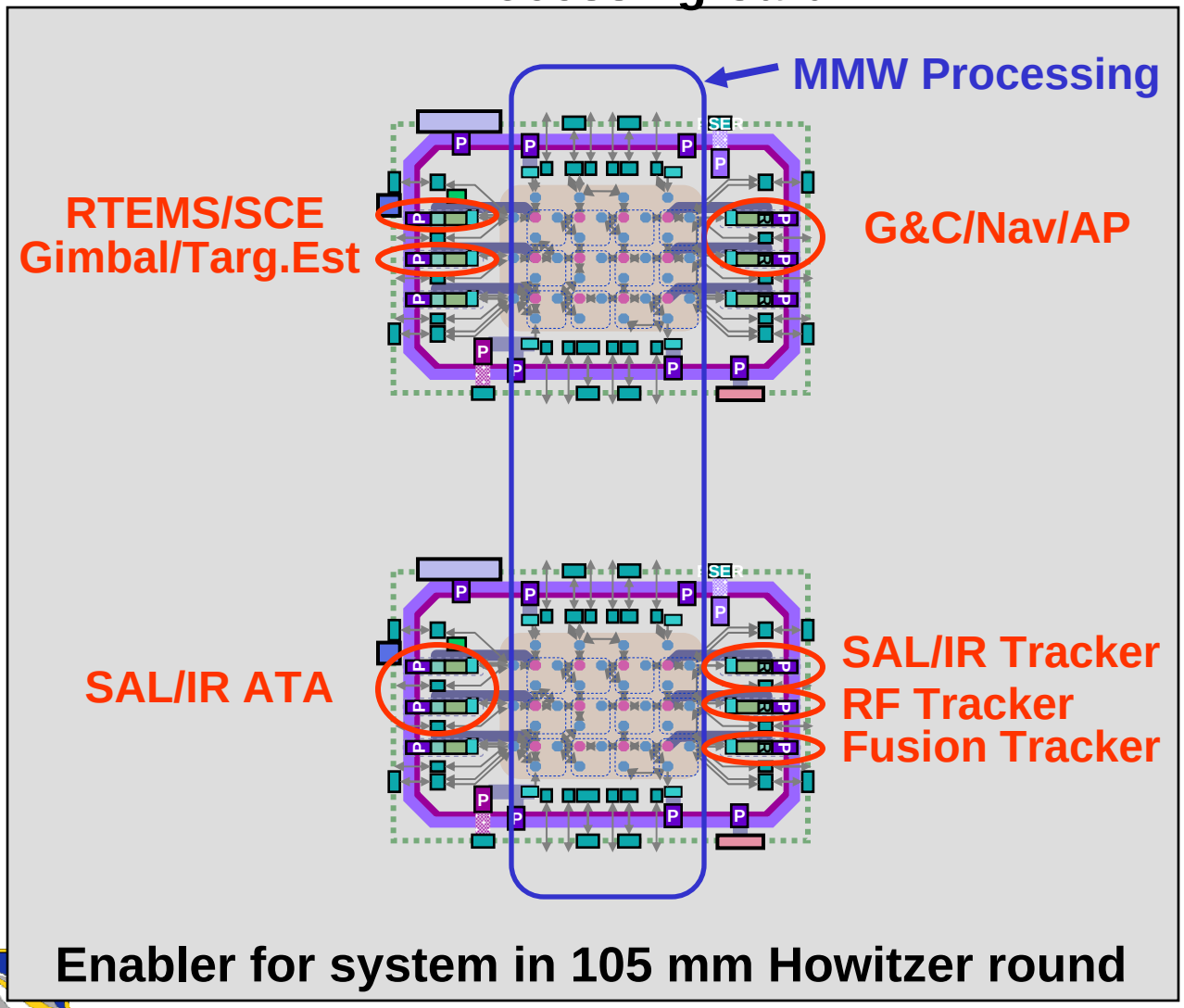
Standard I/O (100 MHz)

DataRate = 12 x 2 GB/s

Example of System on a Chip

Two MONARCH Chips do Full Multi Mode Missile

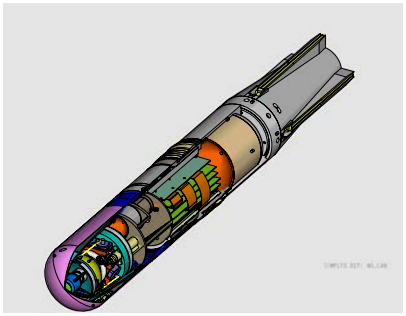
Processing Card



Enabler for system in 105 mm Howitzer round

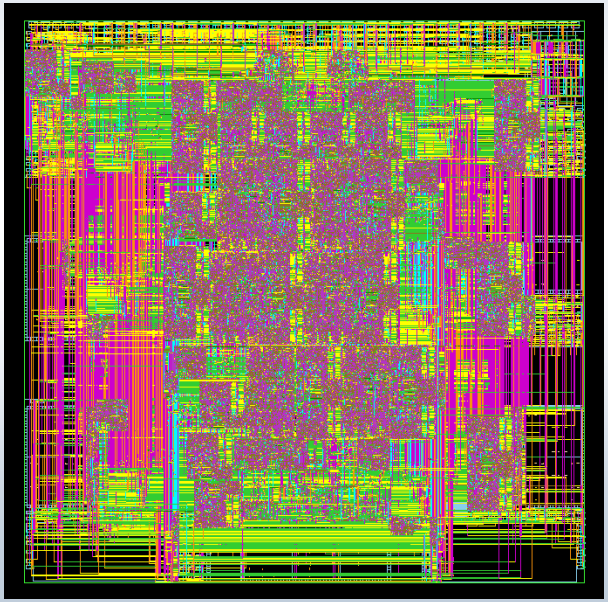
Required Processing

- Millimeter wave radar processing
- Semi active laser
- IR Automatic target recognition
- EO tracker
- RF tracker
- Fusion tracker
- Gimbal and target estimation
- Guidance/control
- Navigation
- Autopilot



MONARCH

Chip Design



March 2006 Full Chip Route

Cu-08 90 nm bulk CMOS
18.76x18.76 mm die
1.5 km wiring
10M nets
282M placeable cells
333 MHz clock
Selective clock gating
8 partition types
Hierarchical design

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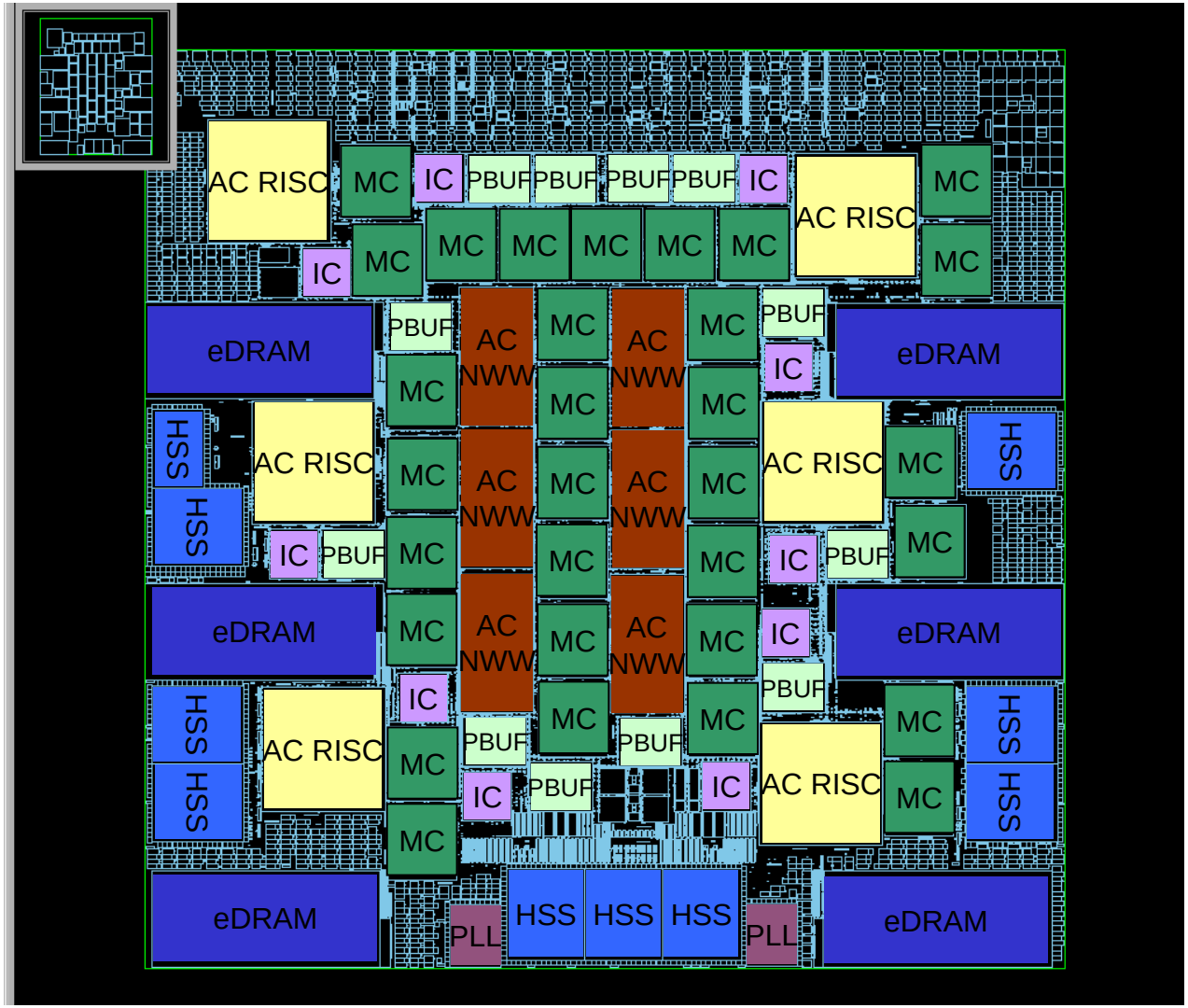
MONARCH – Current Layout

- Standard cell ASIC
- 90 nm bulk CMOS
- 18.76mm x 18.76mm
- 1059 signal I/O
- 333 MHz
- 16 - 31- 42W



- AC – Arithmetic Cluster
- ACNWW – AC without RISC
- AC RISC – AC with RISC and wide word
- HSS – High Speed Serial I/O
- IC – I/O Cluster
- MC – Memory Cluster
- PBUF – Parcel Buffer
- PLL – Phase Lock Loop

MONARCH

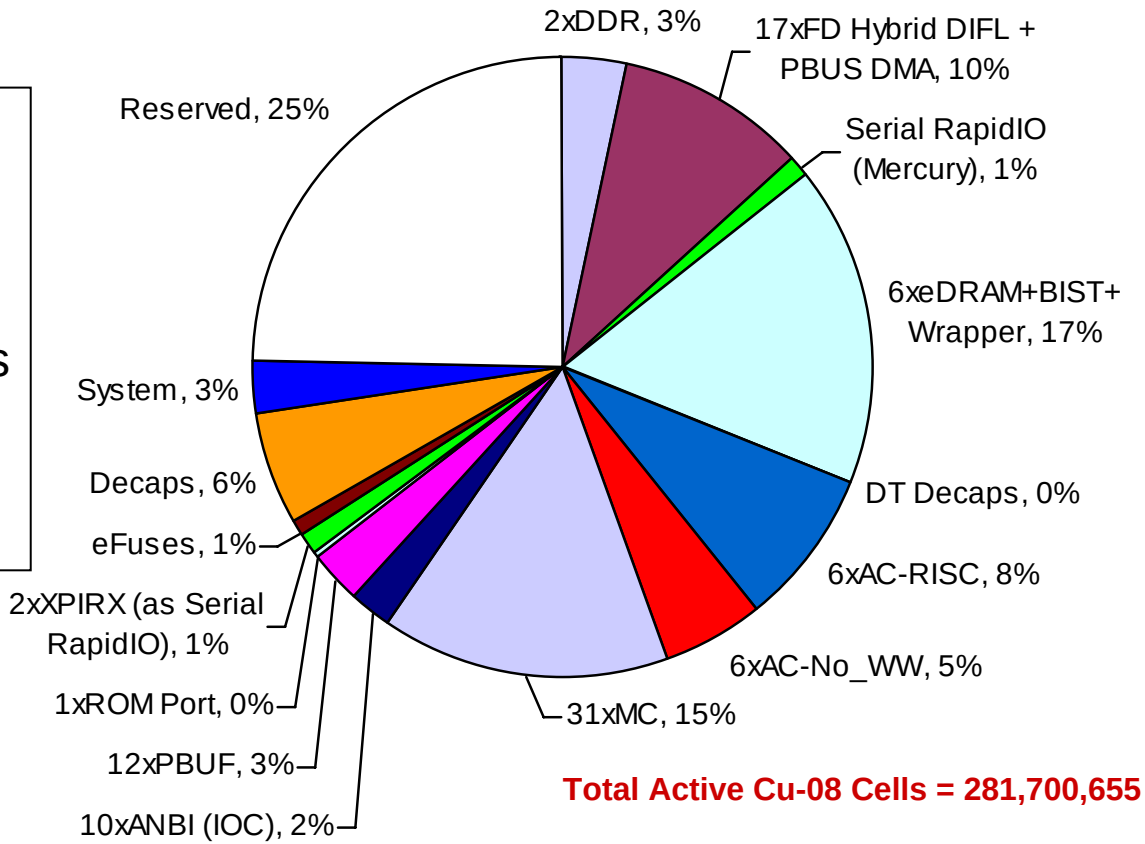
ASIC Area Breakdown
Full MONARCH chip

Physical design indicates good design fit; design fit is stable

Based on IBM's max die size of 352sq mm (18.76mm on a side)

Full functionality Chip

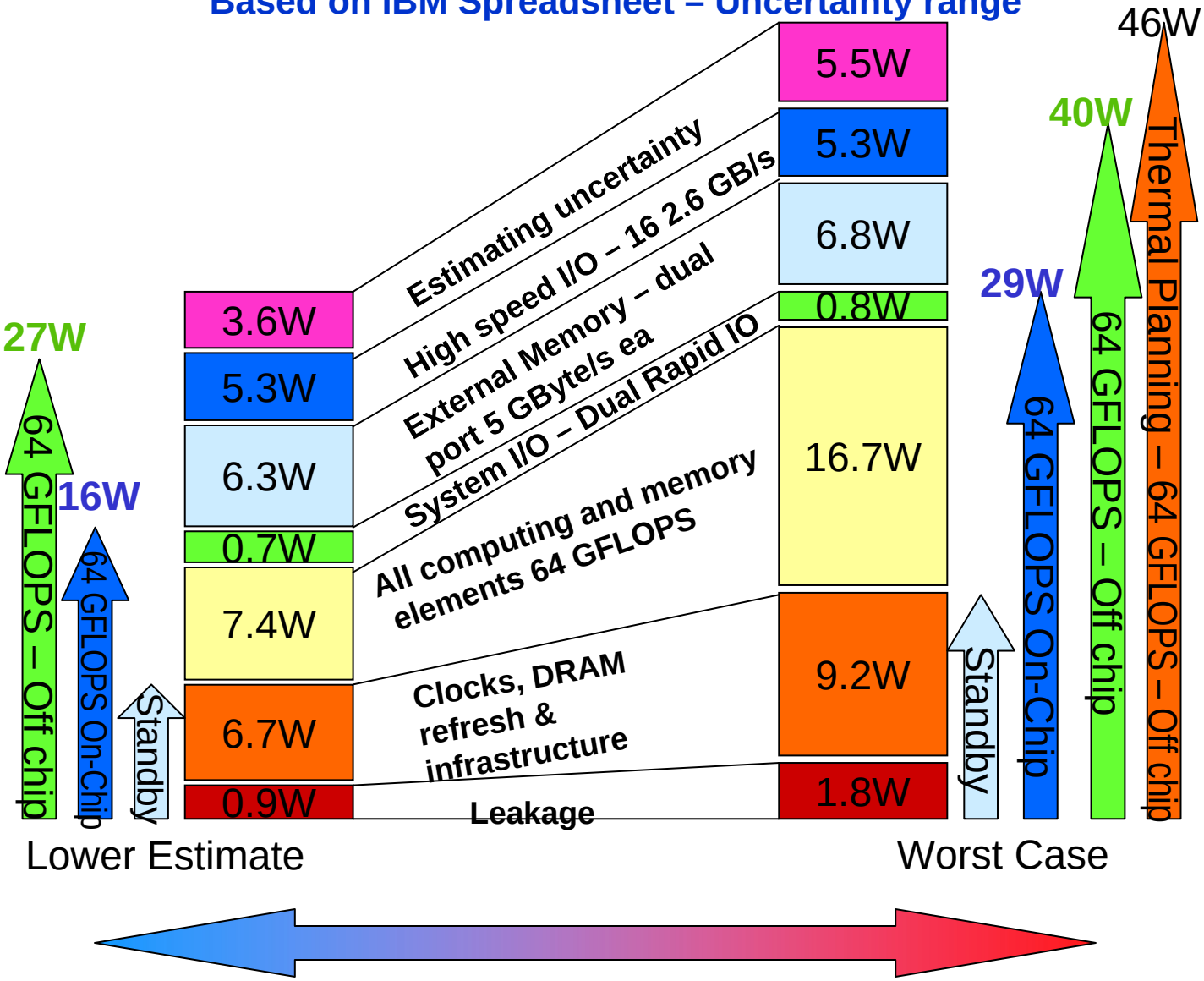
- 6 RISC
- 12 MBytes RAM
- 3x4 tile array
- 16 high speed I/O ports
- 2 serial RapidIO ports
- 2 ext memory ports



Total Active Cu-08 Cells = 281,700,655

MONARCH Power Estimates

Based on IBM Spreadsheet – Uncertainty range



Uncertainties: activity factors, power estimating rules

MONARCH Transition Opportunities

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Application Plans

- **Multiple potential transition users**
  - GPS single or dual chip embedded AJ + modes
  - Space RF/EO applications – front end processing + modes
  - Airborne radar – beam forming
  - ATR – F18 – recognition algorithms
- **Common interest and decision points are:**
  - Performance (throughput, memory, and I/O)
  - Power and performance per Watt
  - Software development environment
- **Rad hard community initiated independent reviews to assess hardening feasibility**

Summary

- MONARCH processor provides high efficient embedded computing
  - Software development station available now
  - Chip in emulation/fabrication now
  - First silicon December 2006
- Boards and demonstrations available in 2007
  - Transition evaluations underway
    - GPS antijam, software defined radio
    - Airborne wide band radar
    - Space applications EO/RF
    - Airborne ATR
- Seeking additional transition programs
  - To ensure technology investments are actively used