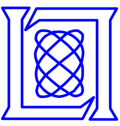
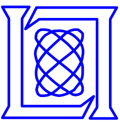




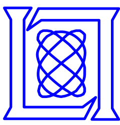
# New Process Technologies – *Will silicon CMOS carry us to the end of the Roadmap?*

**Craig L. Keast, Chenson Chen, Mike Fritze,**
**Jakub Kedzierski, Dave Shaver**



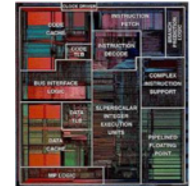
# Outline

- A brief history of CMOS scaling
- Drivers behind “Moore’s Law” and their future outlook
- The potential of “Next Generation” technologies beyond silicon CMOS
- Some comments on 3D circuit integration
- Summary

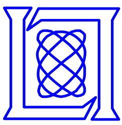


# A Few Metrics

- **Vacuum tube (early 1900's) – transistor (1949) – integrated circuit- IC, "chip" (1959)**
  - **During the first 10 years of the chip's development the US government bought the majority of all ICs produced**
  - **Today the US Government purchases are a few percent of the market**

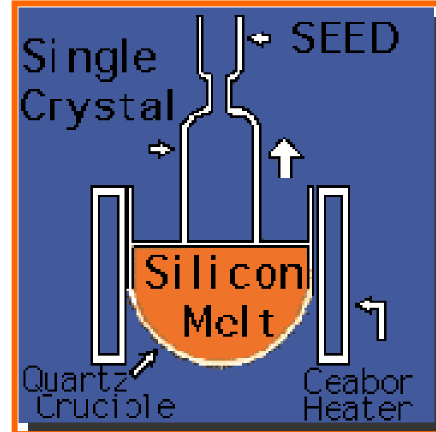


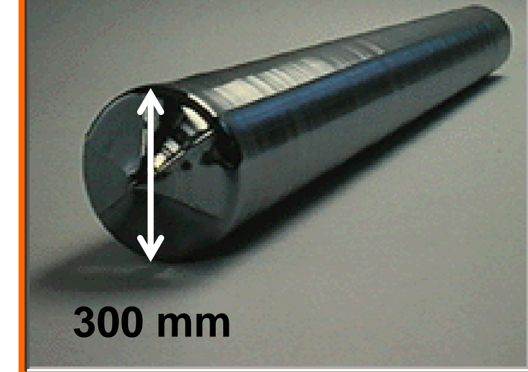
- **Today's microprocessors contain >500 million transistors and occupy ~2-3 $cm^2$ area**
  - **Equivalent number of vacuum tubes would cover an area equal to ~250 football fields**
- **First ICs cost ~$120 and contained 10 transistors ($12/transistor), today's microprocessors cost ~$500 and contain 500,000,000 transistors ($0.000001/transistor)**
  - **If this cost scaling was applied to the automobile industry a $100,000 Porsche 911(turbo) would now cost < 1 cent**

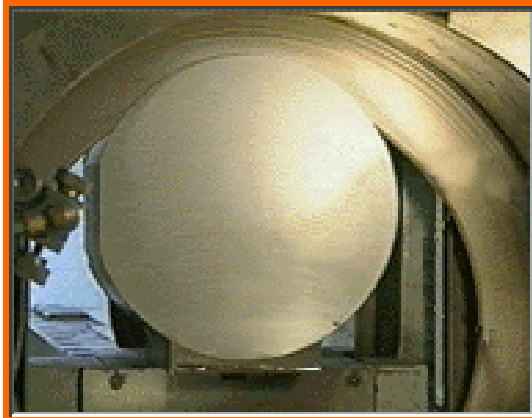


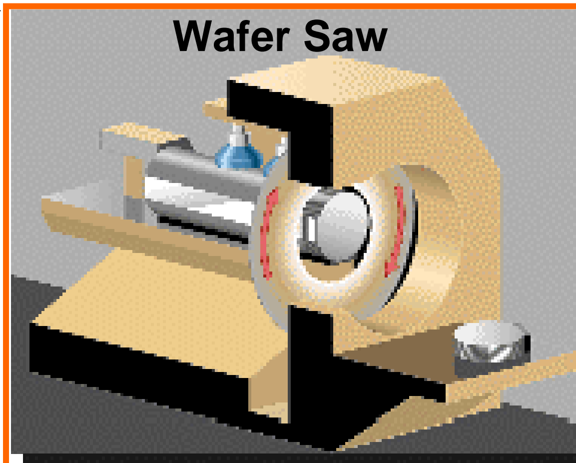
# Silicon – The Material Enabling the IC

## (Semiconductor Wafer Preparation)



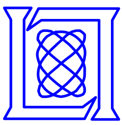









*Silicon's Oxide ($SiO_2$) is a KEY attribute of this material's success*



# 35 Years of CMOS Scaling and Process Improvements

IC cross section

Backend

Frontend

10 μm

1 μm

100 nm

10 nm

1 nm

Technology Node

Self-Aligned Gates

Self-Aligned Silicides

CMP

Tungsten Plugs

Halo Implants

Copper Interconnect

Low-k Dielectric

Strained Silicon

High-k Dielectric???

CMOS Replaces Bipolar
For High Performance Computing

CMOS Starts to Replace
III-V for Some RF Applications

Presumed Limit
to Scaling

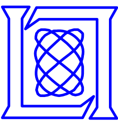
Bulk Silicon

SOI

????

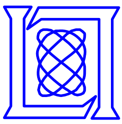
1970 1980 1990 2000 2010 2020

Year



# Drivers Behind Moore's Law

- Smaller feature sizes
  - Pack more features in given silicon area
    - Lower cost per function
  - Smaller transistors are faster
  - Smaller transistors and wires consume less energy
- Bigger chips
  - More functions on one chip reduces packaging and integration costs, reduces power, improves reliability
- Bigger wafer sizes
  - More chips per wafer; wafer processing cost for bigger wafers rises more slowly than number of transistors/wafer
- Manufacturing know-how
  - Faster machines, higher yields, better tool utilization
- More clever device, circuit, and process design
  - Pack more in a given area, even for a given feature size
  - "Equivalent scaling": next generation performance through improved process/materials: SiGe, SOI, strained silicon



# Shrinking Feature Size….

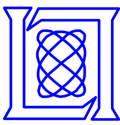
Human Hair

~75 μm

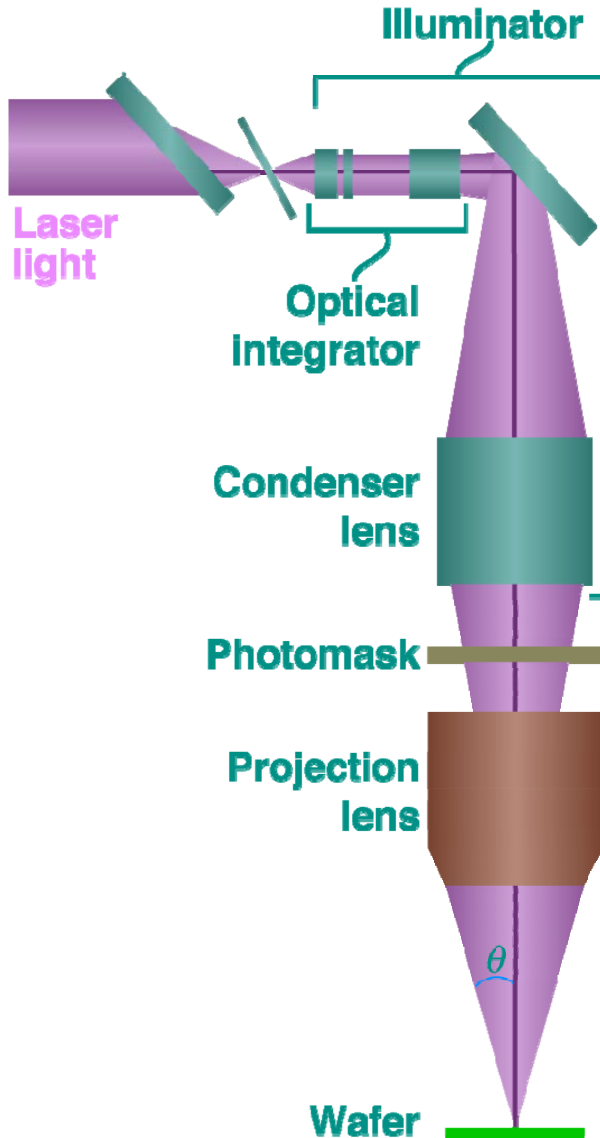
0.18 μm
180 nm
feature

191887-1

*~40,000 (65-nm node) transistors could fit on cross-section*

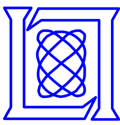


# Lithographic Tools



- Current State of the art (>$25 M)
  - 65 nm resolution
  - $\lambda$ = 193 nm
  - 0.93 NA ($n \sin\theta$)
  - > $10^{13}$ pixels/wafer
  - ~120 300-mm wafers/hour
  - Wafer & mask move 100's of mm/s during exposure

$$W \approx k_1 \frac{\lambda / n}{\sin\theta}$$

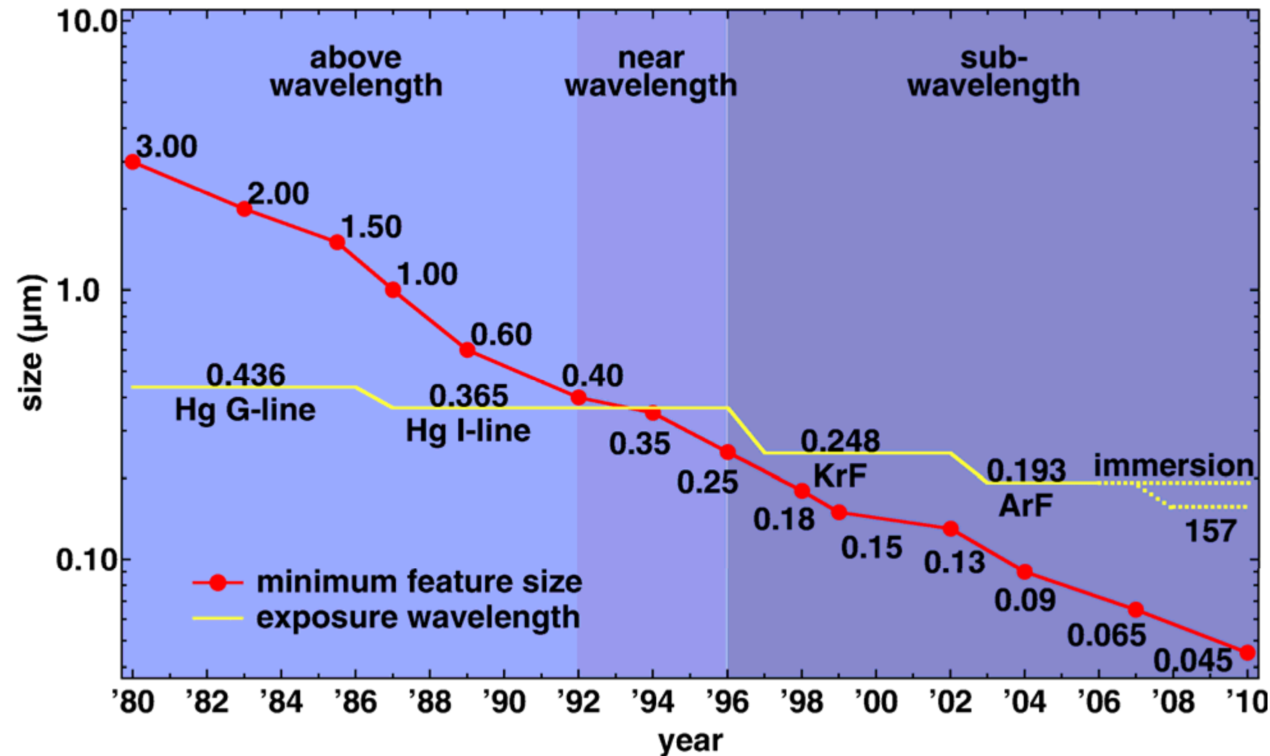


# Optical Lithographic Resolution

- Rayleigh criterion for resolution *W*

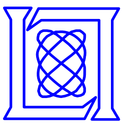
$$W = k_1 \frac{\lambda / n}{\sin\theta}$$

- 30x improvement in resolution over 25 years
  - λ from 436 nm to 193 nm
  - sin θ from 0.35 to 0.93
  - $k_1$ from 0.6 to 0.35
  - *n* from 1 to 1
- Now approaching limits
  - λ limited by materials and sources
  - sin θ < 1
  - $k_1$ > 0.25
  - *n* ???



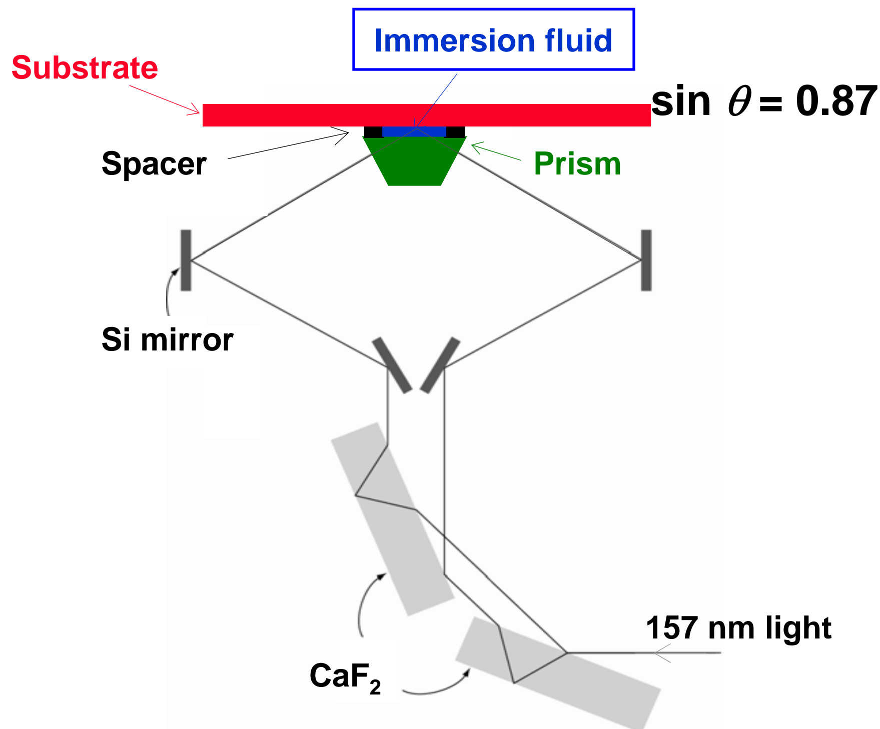


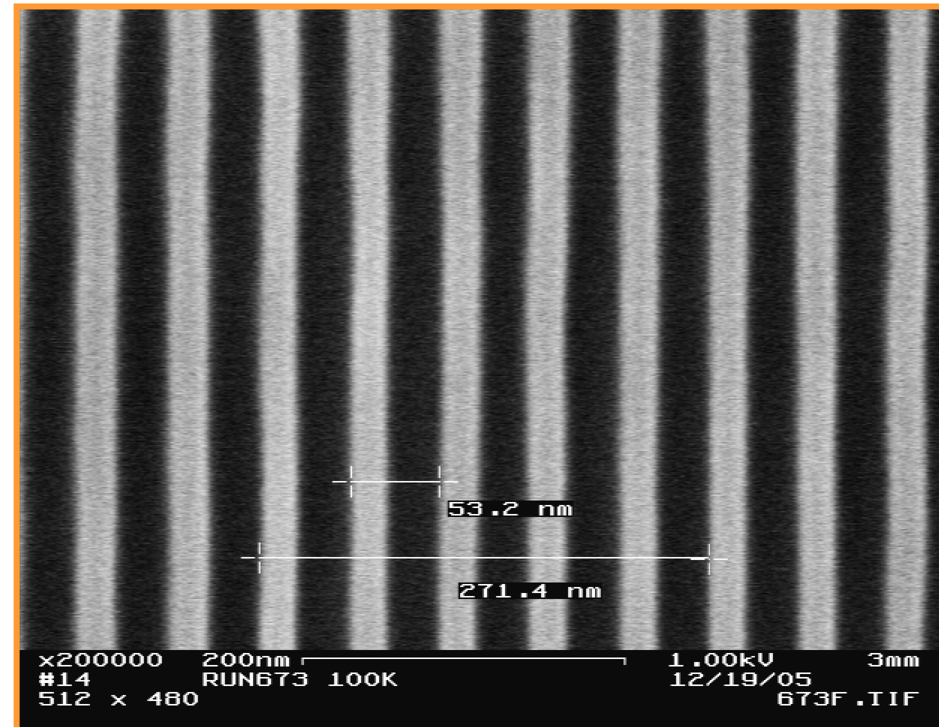

*Slide Courtesy M. Switkes, MIT-LL*



# Liquid Immersion Interference
## *27-nm* Half Pitch

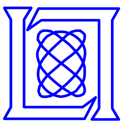
- **High-index fluids** have been designed and synthesized ($n_{157}$ = 1.50)
- Enable coupling of light from prism to wafer
  - No need for solid contact – liquid gap of 2 μm is used



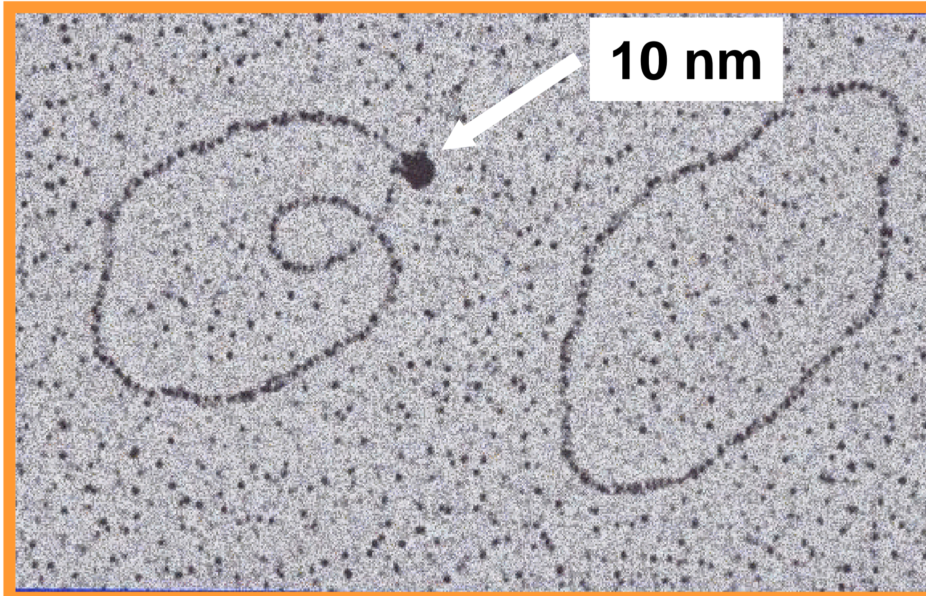



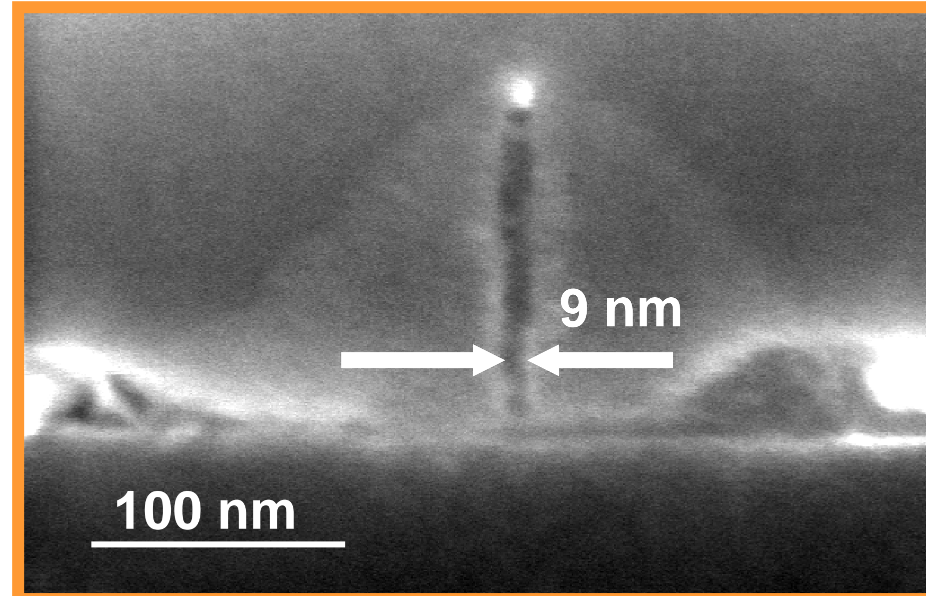



*Slide Courtesy M. Rothschild, MIT-LL*



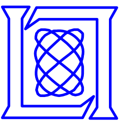
# Optical Lithography at the Nanometer Level



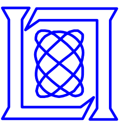

**10 nm gold particle attached to Z-DNA antibody. (John Jackson & Inman. Gene [1989] 84, 221-226)**

**9-nm polysilicon gate on ultra-thin SOI fabricated at MIT-LL using 248-nm PSM optical lithography *(2001)***



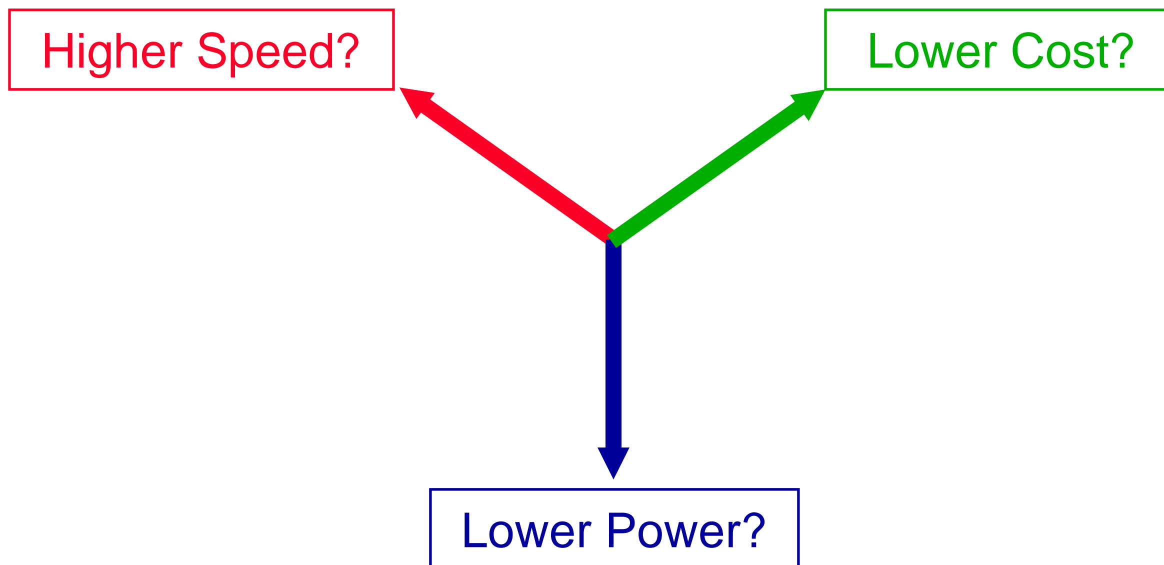
**It is likely that we can pattern the smaller feature sizes needed to maintain CMOS scaling….**

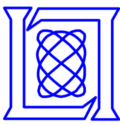
**But will the devices work?**



# Prognosis For Moore's Law Benefits

- **Historically, CMOS scaling has resulted in *simultaneous improvements* in cost per function, circuit (and system) speed, power consumption, and packing density**
- **Will continued scaling give us the same benefits?**





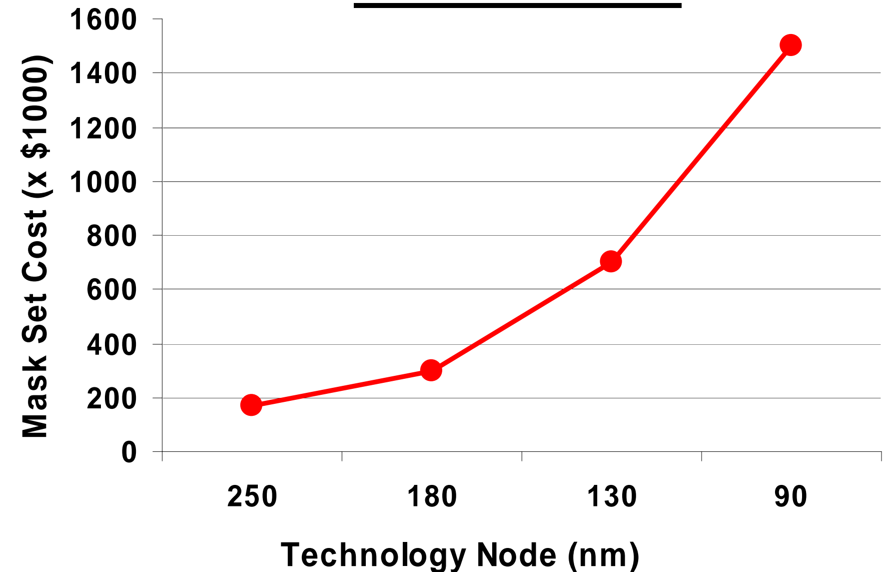
# Lower Cost
# Prognosis For Moore's Law Benefits

**Past**

- Scaling (s) increases components per unit area as $s^2$
- Wafer size increase gives more chips per wafer

⇨ Increasing cost of equipment outweighed by huge increase in number of transistors made per wafer

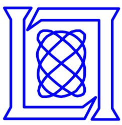
**Mask Set Cost**




**Future Issues**

- Skyrocketing equipment costs…Today's state-of-the-art production facilities cost ~4 billion dollars
- NRE (e.g. >$1M mask sets) and productivity issues favor large volume production of "generic" components
- Increasing consolidation/pooling of fabrication resources and use of Taiwanese "Super Fabs" TSMC and UMC (China and India next?)

⇨ How to get DoD-unique and secure components?



# Lower Power
# Prognosis For Moore's Law Benefits

## Past

- Supply voltage (V) scales as 1/s
- Capacitance (C) scales as 1/s
- Energy per op scales as CV2 ∝ 1/ s3

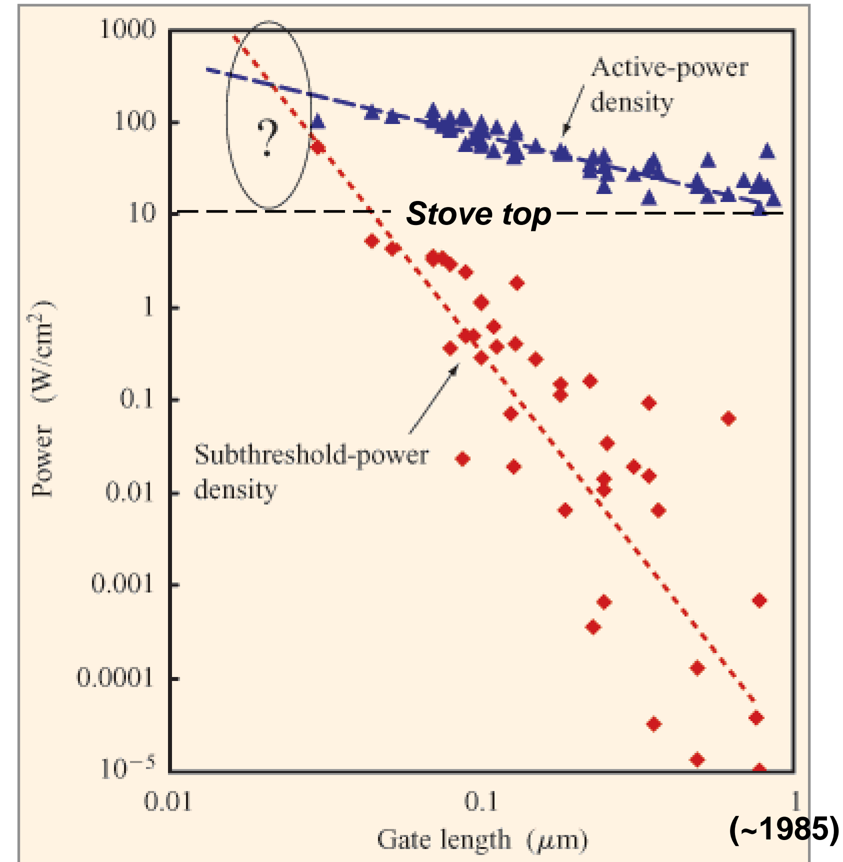
⇨ Voltage scaling from 5V to 1V accounted for 25X reduction in power, just by itself

## Future Issues

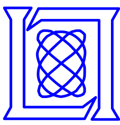
- Power supply voltage only projected to drop 2X over next 15 years (1.0 to 0.5 V)
- Subthreshold device operation?

⇨ Scaling energy per op is critical to long endurance battery powered systems and to supercomputers (getting power in and heat out)

**Passive and Active Power vs Gate Length**

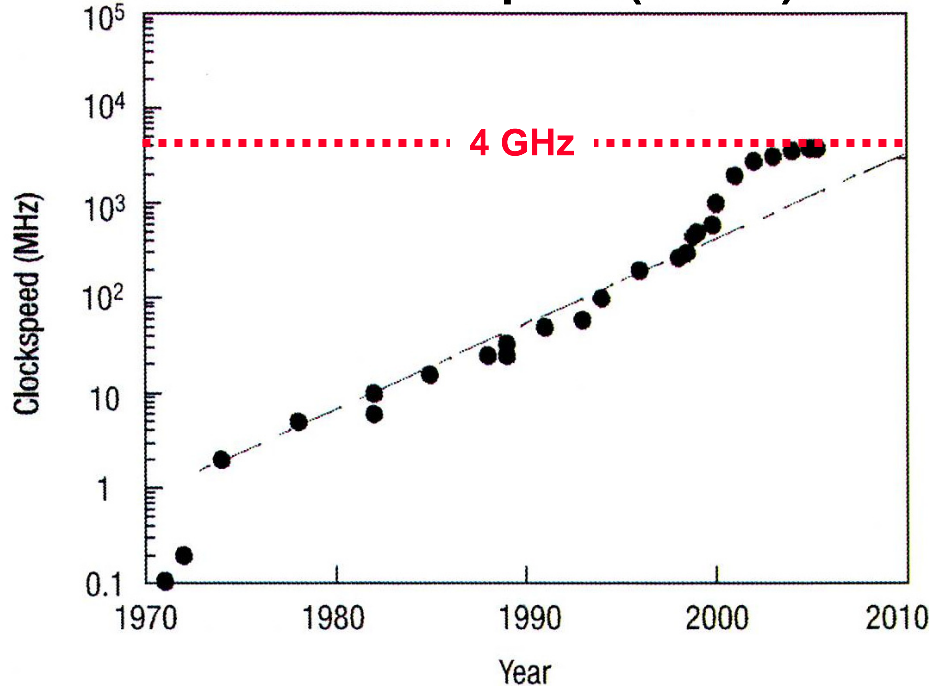



*E. J. Nowak, IBM J. Res. & Dev., Vol. 46, No. 2/3, p. 173*

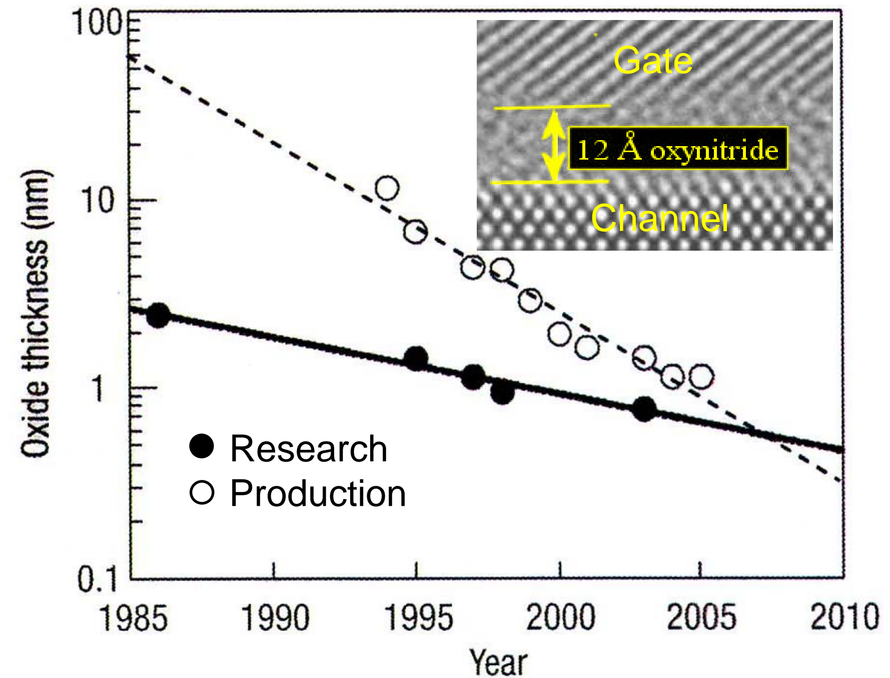


# Higher Speed
## Moore's Law in Trouble

### Processor Speed (INTEL)*



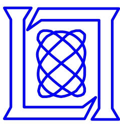

### Gate Oxide Dielectric*




- **CPU speed has stalled for the first time in 35 years, with no processor able to break through the "4-Ghz barrier"**
- **Why?...Gate oxide scaling has stopped at Tox~1.2nm in 2003, at the 90-nm technology node (~3-4 monolayers)**
  - **Only heroic integration efforts, such as use of strained-Si, have made small dents in the CPU speed barrier**
  - **Need a workable High-k gate dielectric in order for performance scaling to continue**

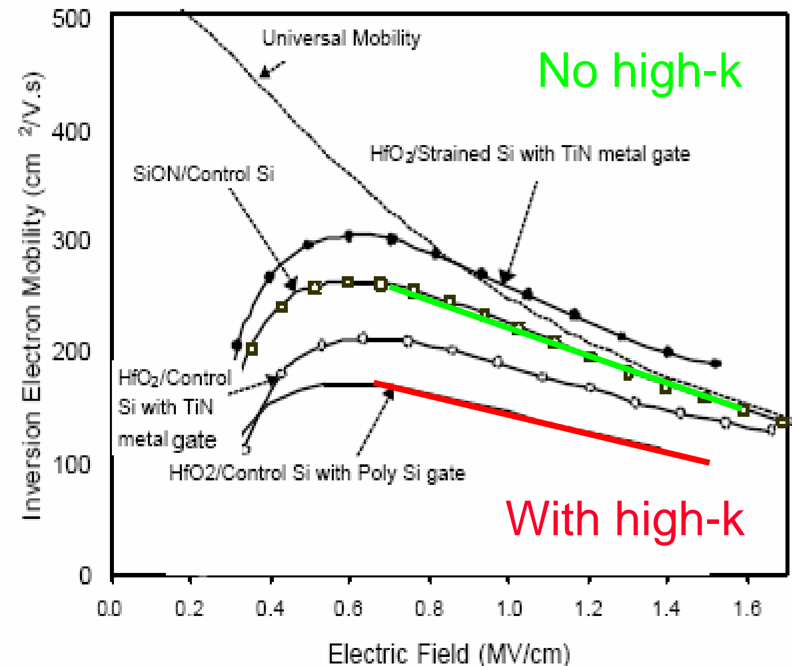


**D. A. Muller, Nature Materials V 4, pg. 645 (2005)*

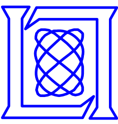


# Future High Performance Device "frontend" Possibilities

- **Continue with Si CMOS. Some possible alternative silicon futures are:**
  - **CPU speed could be maxed out – future improvements will come from reduced cost and higher density and integration**
  - **High-k could save the day – if not tomorrow, maybe in 10 years**
    - **A perfect high-k gate dielectric will enable CPU speeds to increase until the next tunneling limit (source-to-drain) at the 10nm-node**
  - **Changes in device architecture could take the pressure off the gate oxide, and CPU speed will continue to advance at a slower rate**
    - **FDSOI and FinFET lets $T_{si}$ scale instead of $T_{ox}$**



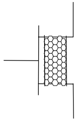

*Intel - components research (IEDM2003)*



# Future Possibilities (Cont'd)

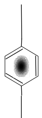
- A future with transistors, but without silicon:
  - Germanium-based devices

    Improved mobility, at the expense of many other semiconductor properties
  - Carbon-based devices. Several flavors:

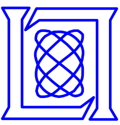


Carbon nanotubes: Have better device properties than Si, but are very difficult to integrate (thus far)

Graphite devices: Difficult to turn off

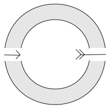


Molecular devices: Have not been demonstrated to work better than Si

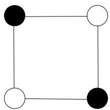


# Future Possibilities (Cont'd)

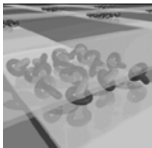
- A future without transistors:



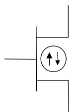
  - Josephson-junction-based logic
    - Demonstrated and works, but at 4K
    - Real speed and power advantages unclear



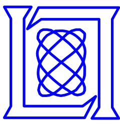
  - Quantum Computation
    - Can't execute traditional code, even theoretically
    - But can solve Schrödinger's equation blazingly fast, and factor very large numbers



  - Cross Point Arrays – nanowire, molecular
    - Too simple for general purpose logic, if complexity is increased to meet logic constraints the result is a transistor



  - MEMS, protein, spin logic – too early to evaluate



# Potential Technology Roadmap

Estimated Performance

Research Required

Silicon devices

Germanium devices

Alternate Si
Structures
FDSOI
FinFET

Perfect high-k

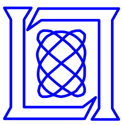
Carbon-nanotube devices

Graphite devices

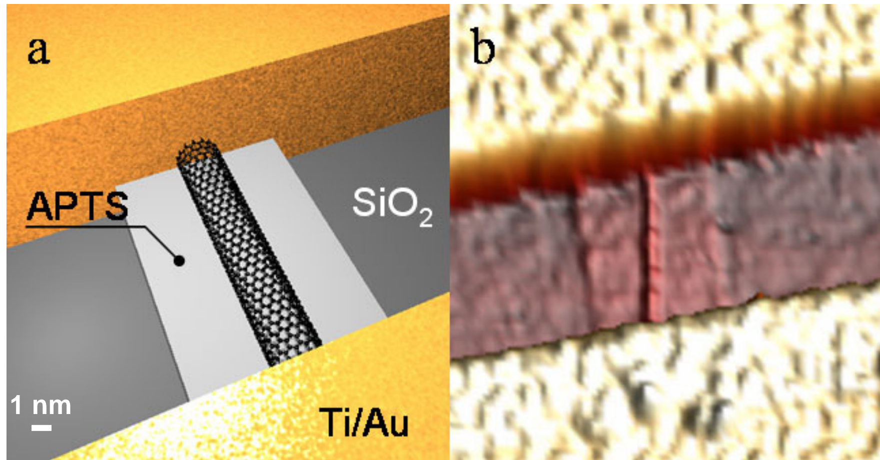
Molecular devices

Spintronics – no evaluation possible, insufficient experimental data

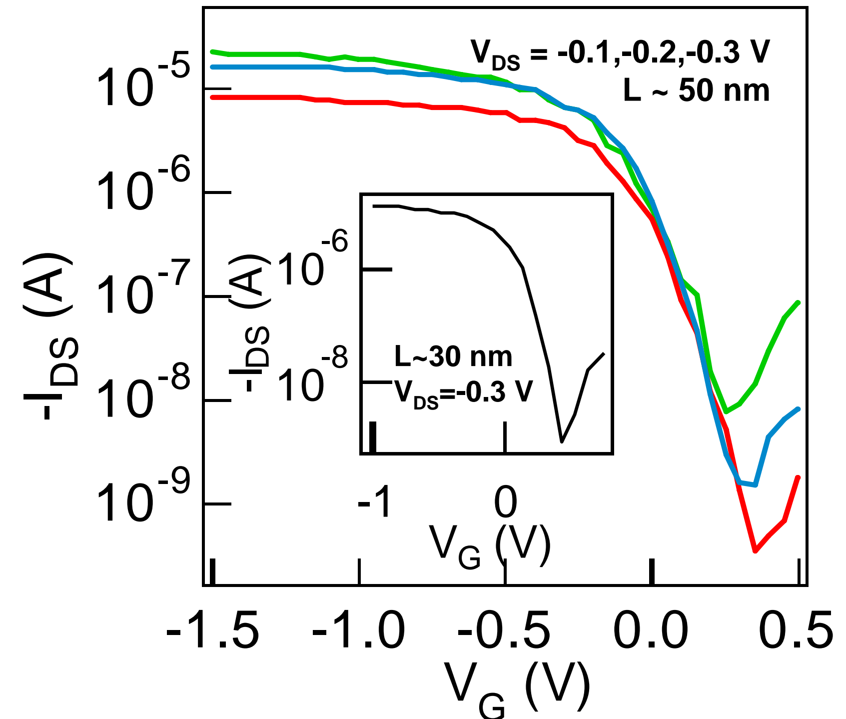
**Possible global directions for high performance logic technology in the next 20 years considered in this study, and graphical summary of their evaluations when possible**



# Future Technology Highlights: Carbon Nanotubes (CNTs)



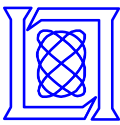

*(Drawing and AFM from CEA website)*



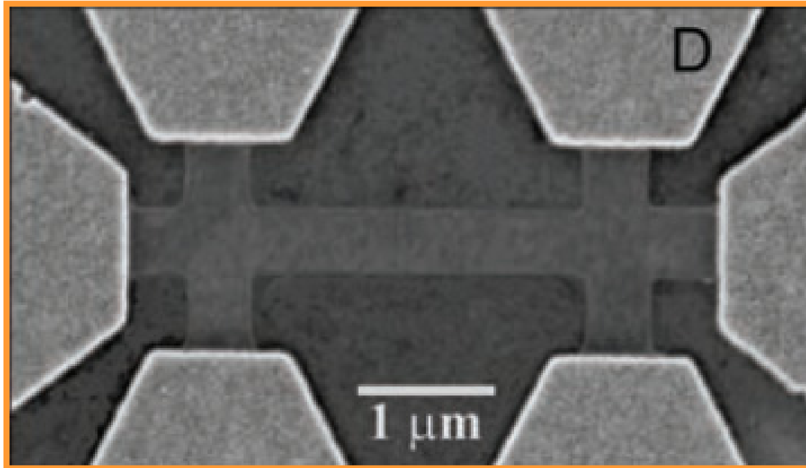

- **Example of experimental CNT device from Stanford**
  - **Features: metal gate, high-k dielectric, metal source/drain**
  - **High performance: 10x Si device of same geometry**
- **Putting tubes were they are needed is a problem**

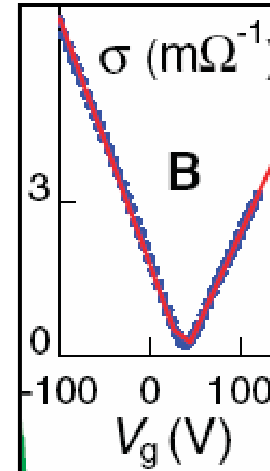


*REF:* A. Javey, et al. Nano Lett, 2004.



# Future Technology Highlights
# Thin Graphite - Graphene

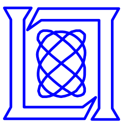



*REF:* K.S Novoselov et al., Science, V. 306, 22 October 2004, p. 666

*Few monolayer graphite device SEM and electrical characteristics at T=70K*

- **Graphite has high mobility of >10,000 cm²/Vs (~15x Si)**
- **Graphite is a semi-metal (semiconductor with band-gap of 0eV)**
  - **Difficult to turn off, a fundamental challenge**
- **Proven planar techniques could be used in fabrication**
  - **Planar geometry of devices eliminates majority of integration difficulties of carbon nanotubes**
- **MIT-LL has begun to explore this material system**
  - **Leveraging layer transfer, materials, and microelectronic fabrication expertise at the Laboratory**



# The Integrated Circuit Interconnect "backend" Challenge

**Relative Wiring Delay vs Feature Size***

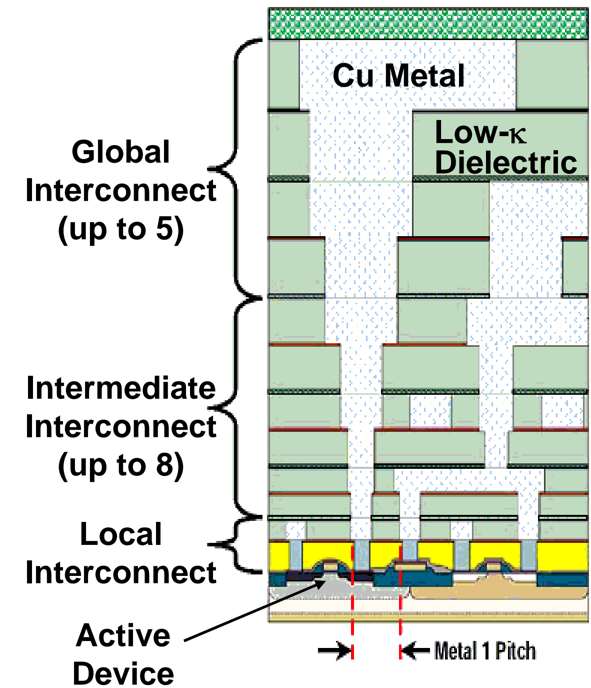
Relative Delay: 100, 10, 1, 0.1

- Gate Delay (Fan Out 4)
- Local Interconnect
- Global Interconnect (w Repeaters)
- Global Interconnect (w/o Repeaters)

250 (1998) | 180 (2000) | 130 (2002) | 90 (2004) | 65 (2007) | 45 (2010) | 32 (2013)

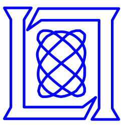
Process Technology Node (nm) (year)

**Typical Process Cross-Section***






*From 2005 International Technology Roadmap for Semiconductors (ITRS)



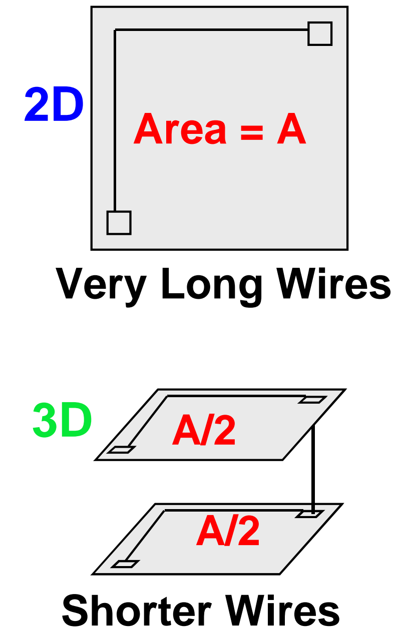
# Wire Length Distribution in 90 nm Node IBM Microprocessor*

Number of Wires

100000
10000
1000
100
10
1

0 to 720
720 to 1440
1140 to2160
2160 to 2880
2880 to 3600
3600 to 4320
4320 to 5040
5040 to 5760
5760 to6480
6480 to 7200
7200 to 7920
7920 to 8640
8640 to 9360
9360 to 10080
10080 to 10800
10800 to 11520
11520 to 12240
12240 to 12960
12960 to 13680
13680 to 14400
14400 to 15120
15120 to 15840
15840 to 16560
16560 to 17280
17280 to 18000

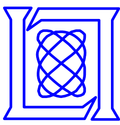
Wire Length (μm)




- >50% of active power (switching) dissipation is in microprocessor interconnects
- >90% of interconnect power is consumed by only 10% of the wires



*After K. Guarini IBM Semiconductor Research and Development Center



# Range of Wire in One Clock Cycle*

From 2003 ITRS Roadmap

Process Technology (nm)

300
250
200
150
100
50
0

1995
2000
2005
2010
2015

Year

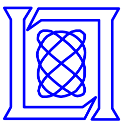
700 MHz
1.25 GHz
2.1 GHz
6 GHz
10 GHz
13.5 GHz

(20 mm x 20 mm Die)

- 3D Integration increases accessible active devices



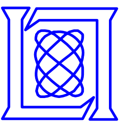
*After S. Amarasinghe, MIT Laboratory for Computer Science and Artificial Intelligence



# Cross-Section of 3-Tier 3D-integrated Circuit

## 3 FDSOI CMOS Transistor Layers, 10-levels of Metal

Tier-3: Transistor Layer
Back Metal
Tier-3: 180-nm, 1.5V FDSOI CMOS
Stacked Vias
3D-Via
Metal Fill
Oxide Bond Interface
Tier-2: Transistor Layer
3D-Via
Tier-2: 180-nm 1.5V FDSOI CMOS
3D-Via
3-Level Metal
Oxide Bond Interface
Tier-1: Transistor Layer
Tier-1: 180-nm, 1.5V FDSOI CMOS
10 μm



# Summary

- Transistor feasibility has been demonstrated to below ~10 nm gate lengths
- "Conventional" CMOS (Bulk, $SiO_2$ gate oxide, poly gates) faces significant challenges to scale below 45nm-node
  - Ultra-thin-body SOI, FinFET, Dual-Gate, Metal Gate, High-k
  - No new device technology has yet emerged that is expected to dethrone silicon CMOS
- Moore's Law scaling is showing its age and could run into serious speedbumps in the next few years (including economics), but the 2020 roadmap is theoretically feasible
  - Process technology improvements are no longer the performance drivers
- Future performance improvements will most likely come through circuit, system architecture, and software advancements