C-Based Hardware Design Platform for Dynamically Reconfigurable Processor

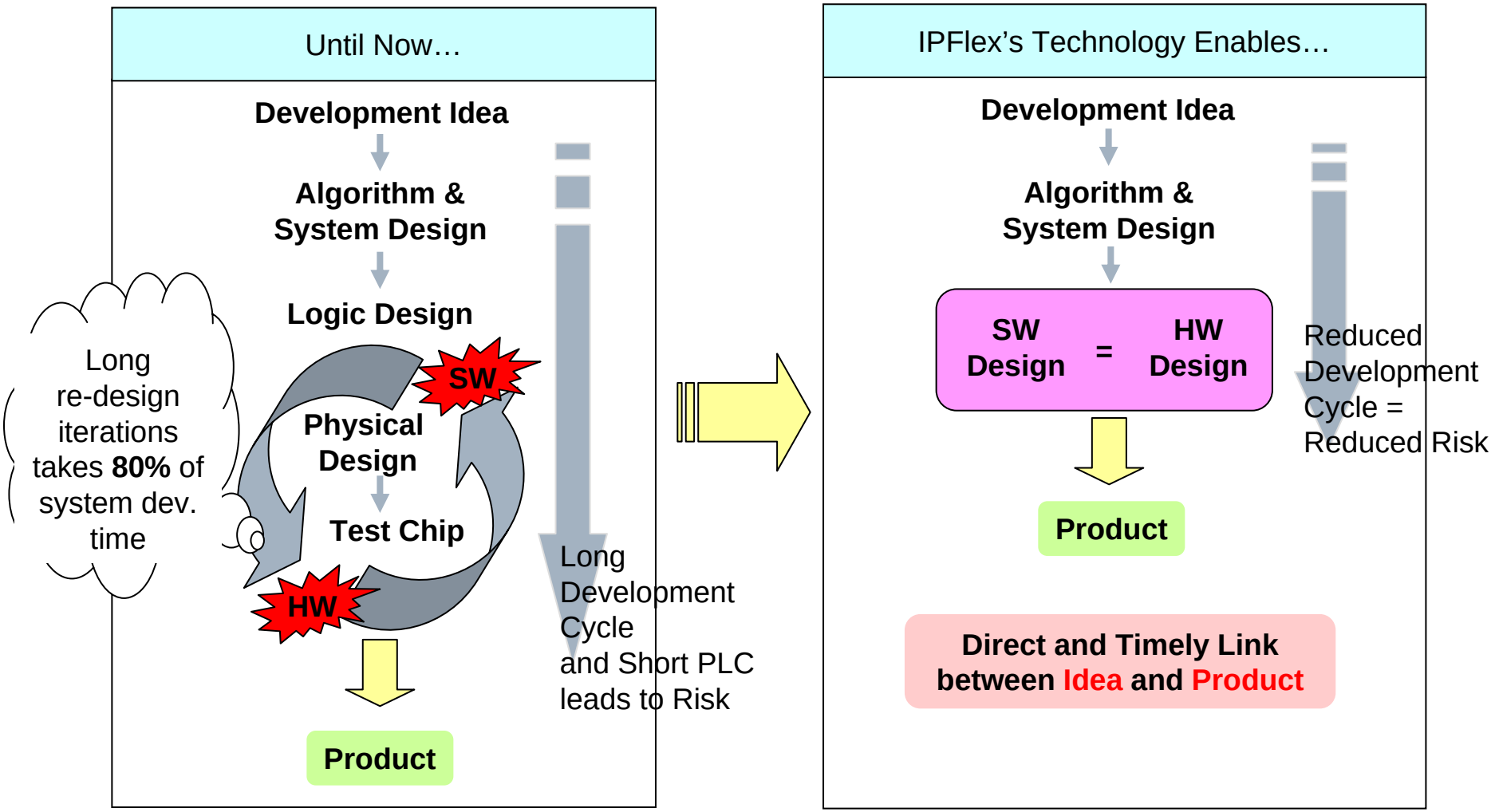
September 22nd, 2005

IPFlex Inc.

Agenda

- **Merits of C-Based hardware design**
- **Hardware enabling C-Based hardware design**
- **DAPDNA-FW II Design Tool**
- **Programming Example and Performance**

Short development iteration while achieving high performance



HW and SW enabling short iteration cycle

Dynamically Reconfigurable Hardware

Hardware functions reconfigured in a single clock

Software to Silicon™

Hardware design with C-like language

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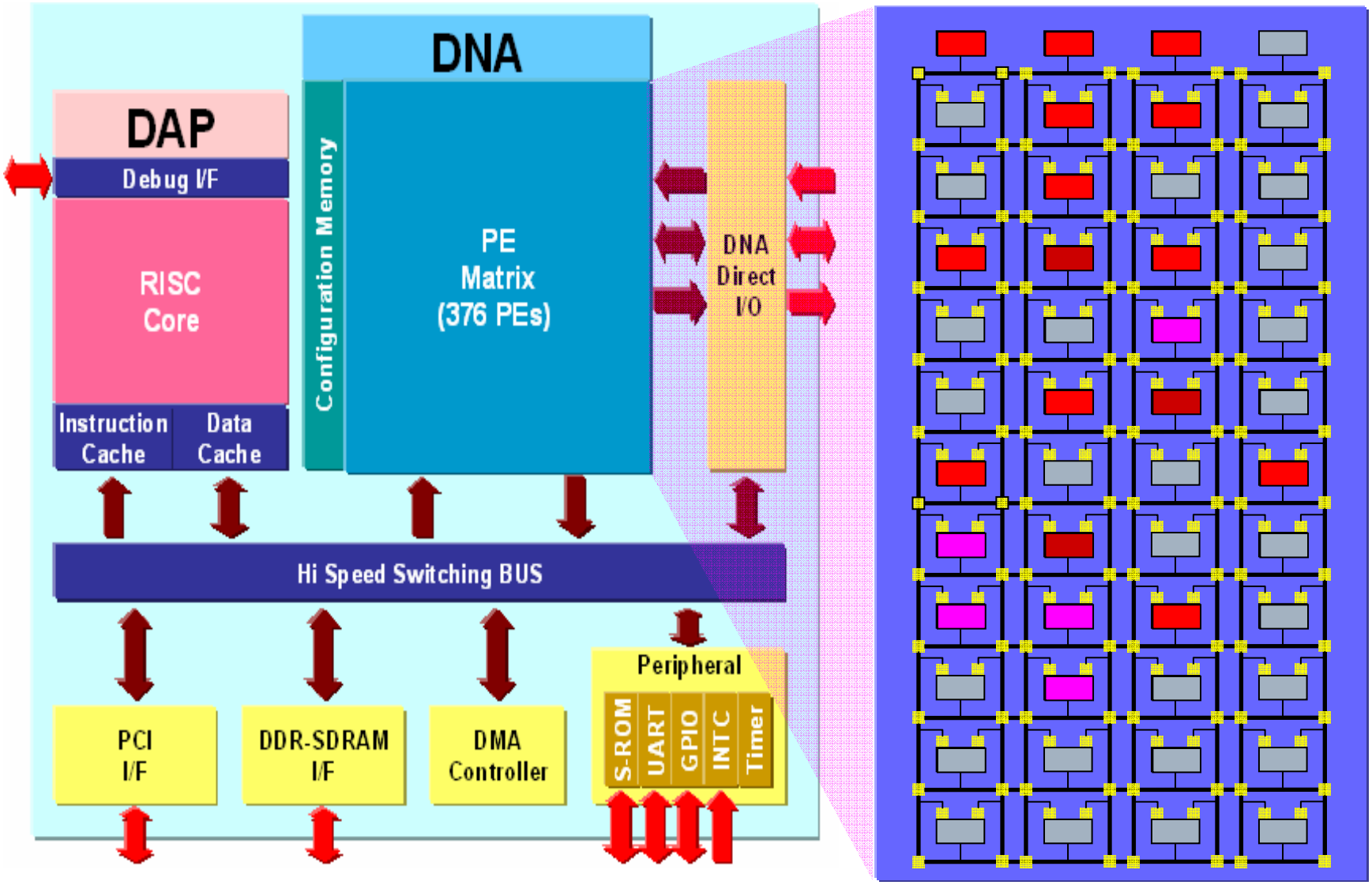
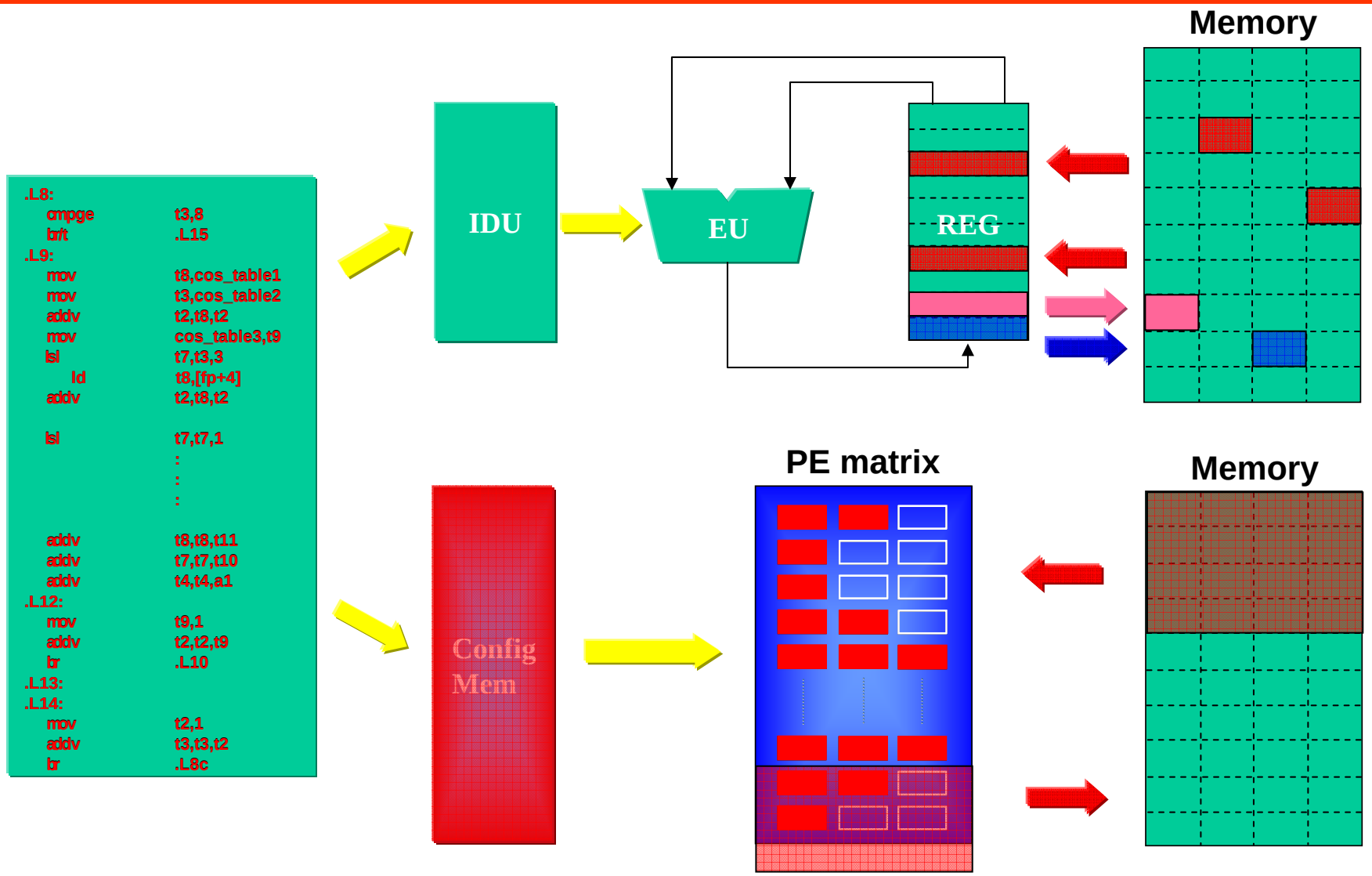
RISC core and dynamically reconfigurable data flow machine

- 166MHz
- 376 32 bit processing elements
- 512KB Internal RAM
- Direct I/O
- DDR SDRAM
- Processor chip, design tool, evaluation boards available

RISC core and dynamically reconfigurable data flow machine

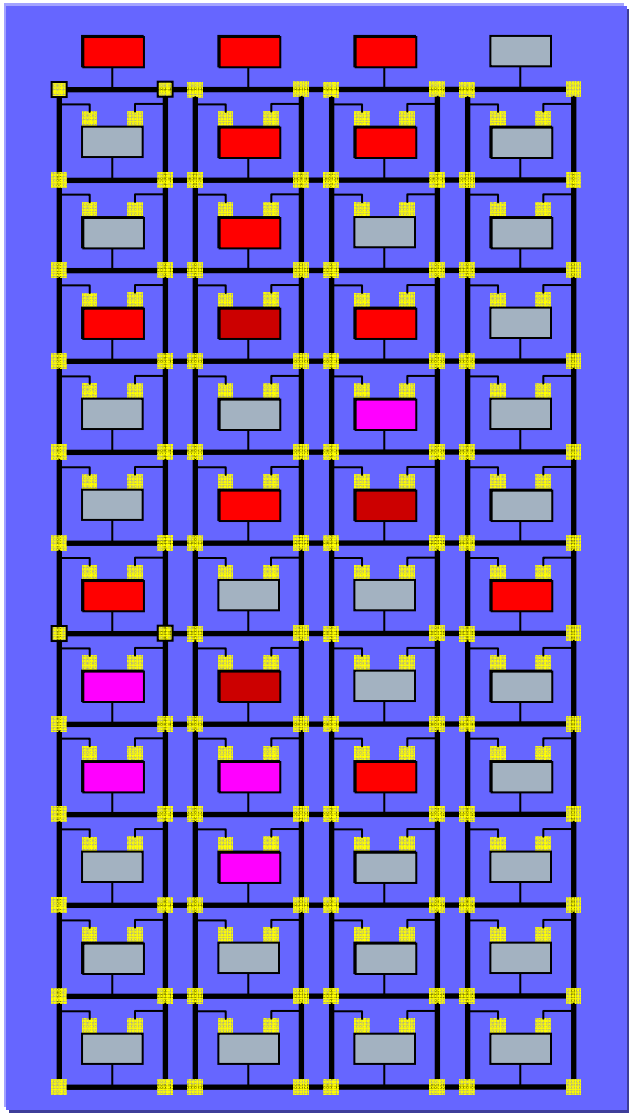


DAP RISC and DNA Parallel Data Processing



Heterogeneous PE Matrix

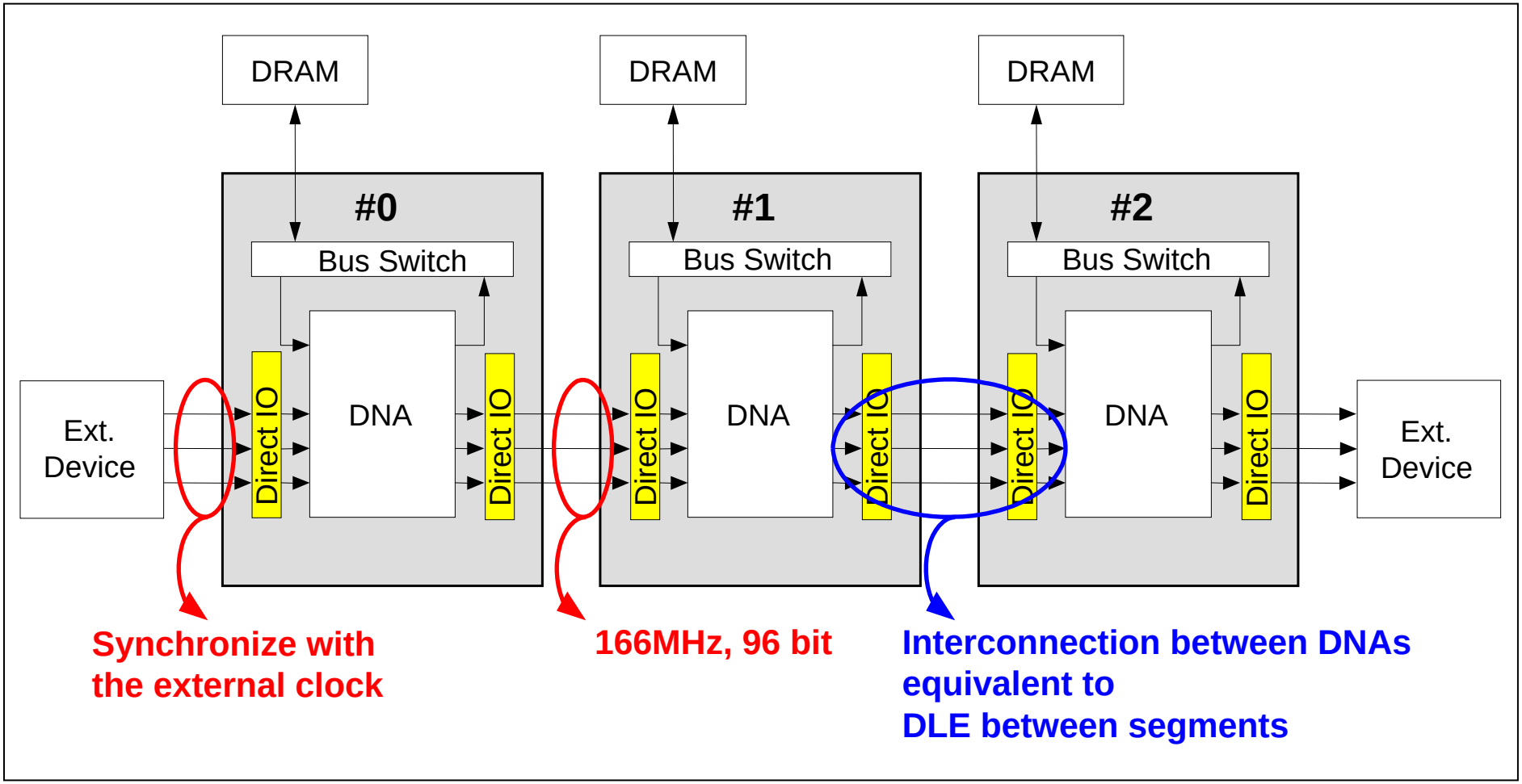
PE Matrix



PE	#	Functionality
EXE **EXM**	**112** **56**	• 32 bit 2 inputs / 1 output execution elements • 16bitx16bit->32bit multipliers
DLE	**136**	• 32 bit 2 inputs / 1 output delay element
RAM	**32**	• DNA Internal memory element • 16KB×32 =512KB
C16E **C32E**	**24**	• Address generators
LDx **STx**	**16**	• I/O buffers
Total	**376**	

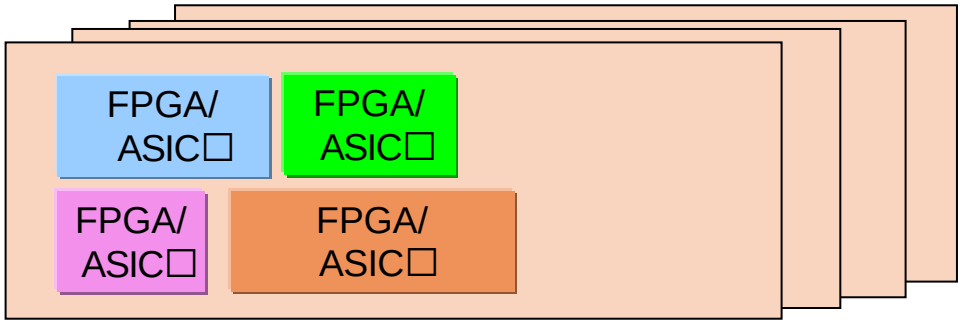
Scalability with DNA Direct I/O

16 DNAs at 16Gbps flow-thru (Total 32 Gbps I/O)



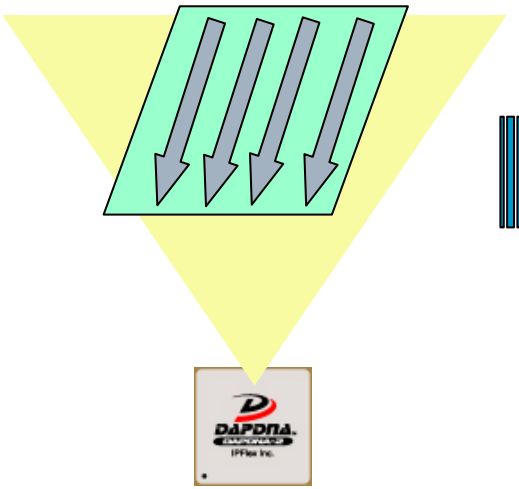
DAPDNA architecture: solution at any system size

System Example



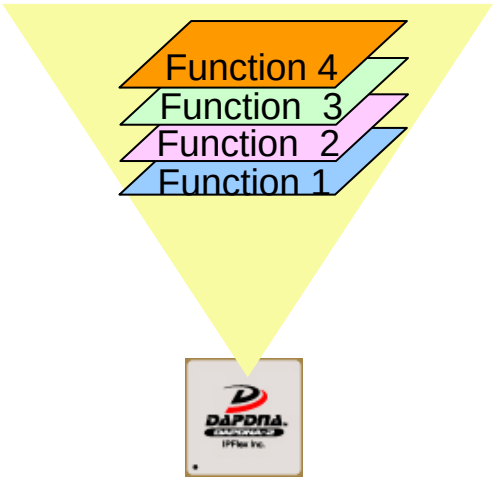
4 Pipelined Processes | **Dynamic Reconfiguration** | **Scalability**

Small scale



[One DNA Plane]

Mid/Large size



[One DAPDNA Processor]

Ultra large

[Up to 16 DAPDNA Processors]

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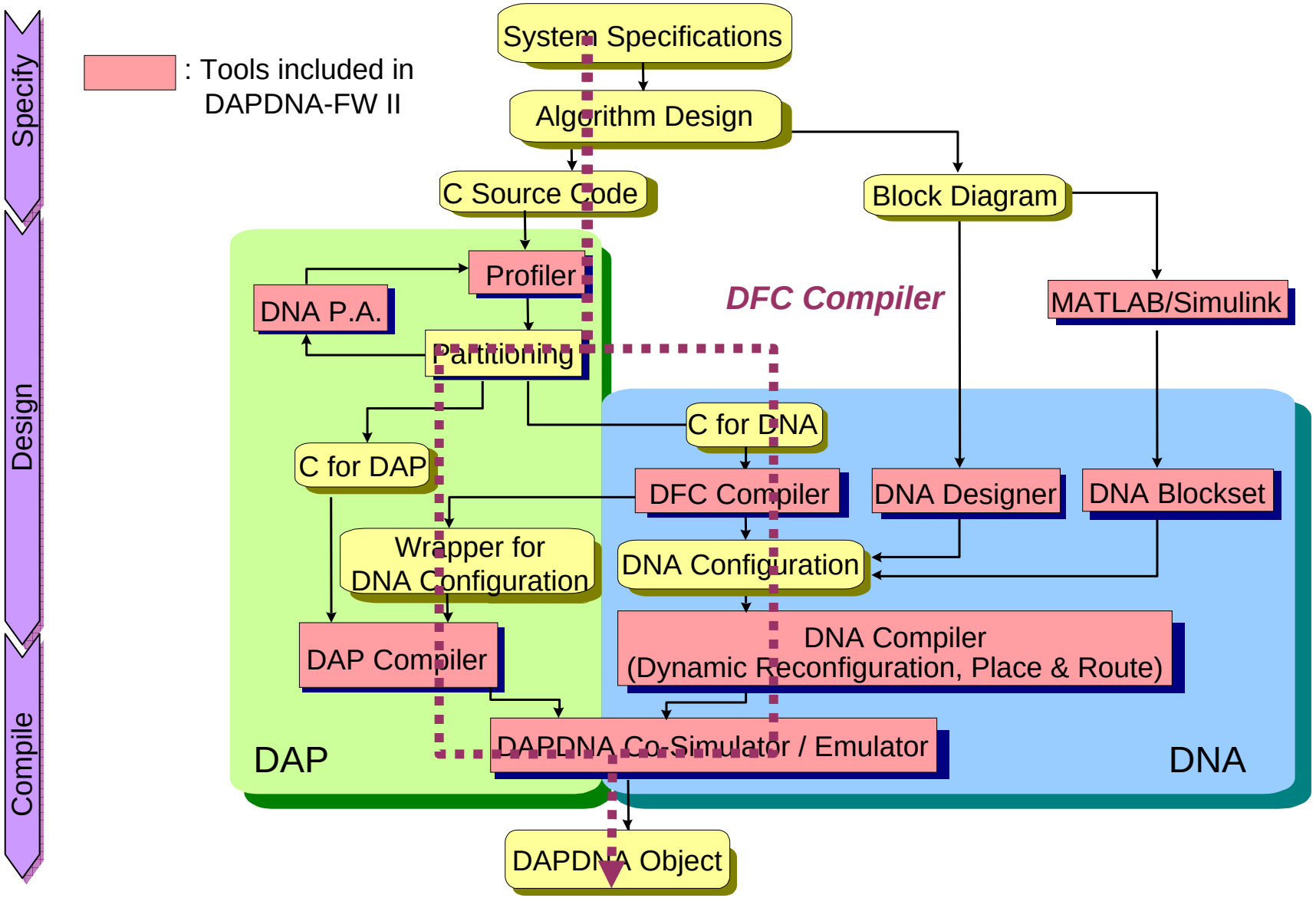
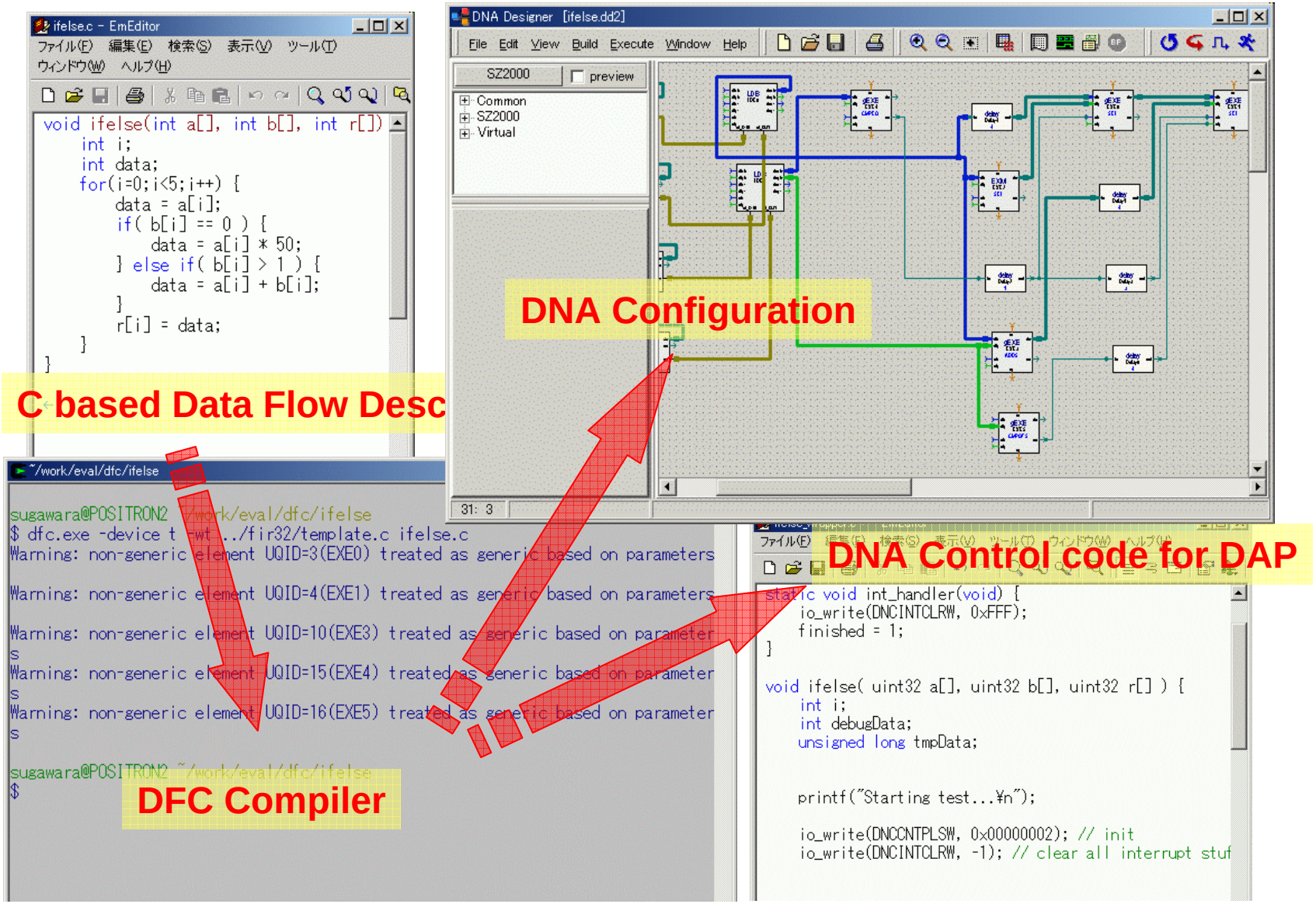
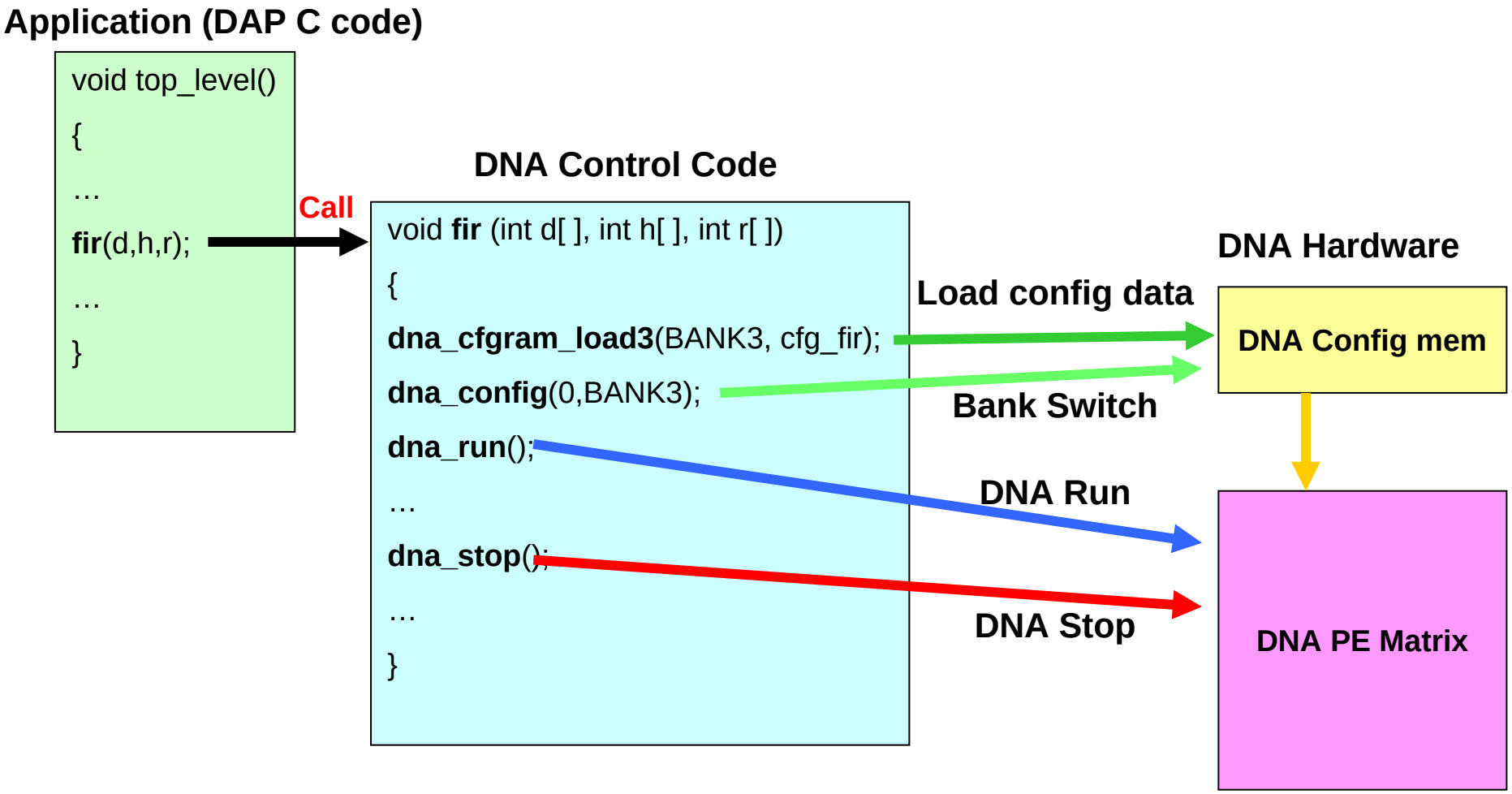
Data Flow C compiler: A part of Software to Silicon design tool



DFC Compiler: HW configurations from C language



HW configurations written in DFC as functions

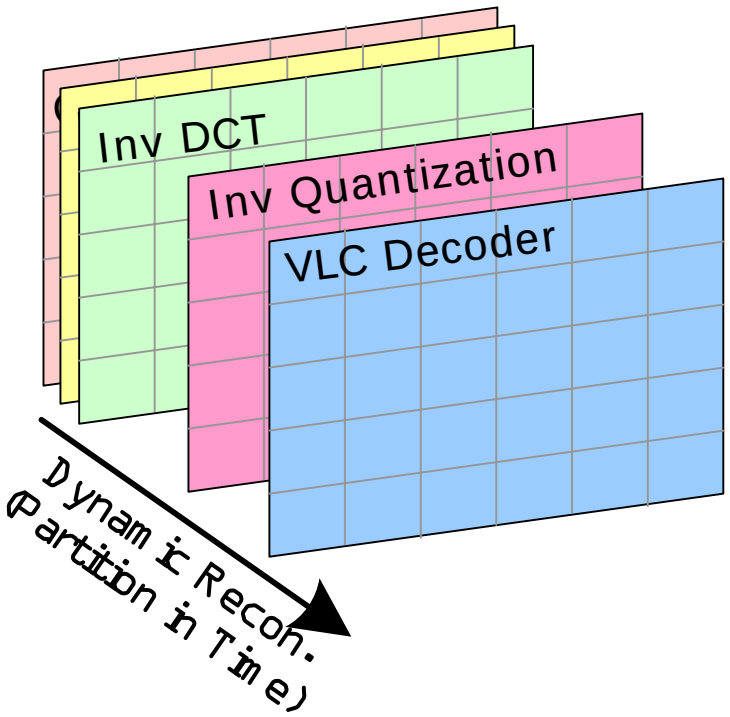


HW configurations switched dynamically in single clock (6 nano second)

Application (DAP C code)

```
...
while (1) {
  ...
  VLC_Decoder(Vector,Quant_dat,Input);
  Inv_Quantize(dct_dat, quant_dat);
  Inv_DCT(mc_dat, dct_dat);
  Motion_Comp(mcu_dat,mc_dat);
  Color_Conv(mcu_dat, mcu_dat);
  ...
}
```

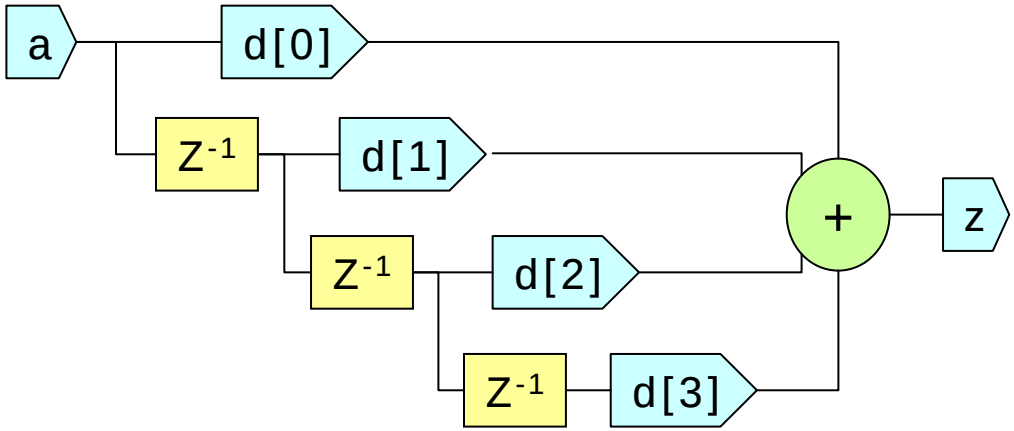
DNA Hardware



Extension on ANSI C for data flow systems

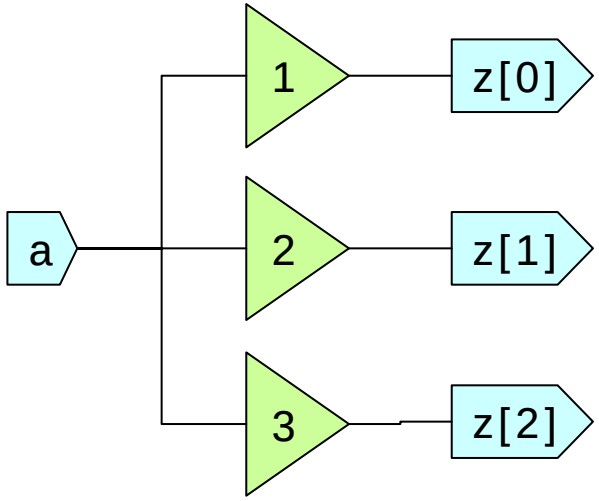
- **Delayline: delayed data signals**

```
delayline d;
d = a;
z = d[0] + d[1]
    + d[2] + d[3];
```



- **SEQ: Static code replication**

```
int h[] = {1,2,3};
int z[];
seq (i=0; i<3; i++) {
    z[i] = a * h[i];
}
```



Advantages of DAPDNA architecture

- **Short development period**
  - Rapid prototyping
  - Co-Simulation between Processor (DAP RISC) and Data Flow Machine (DNA PE Matrix)
  - Deterministic placement / guaranteed clock speed @ 166Mhz
- **Flexibility to change HW according to the application in demand**
  - Dynamic reconfiguration in single clock
- **Performance close to custom device**
  - Deep pipelining and massive parallelization
  - 376 processing elements

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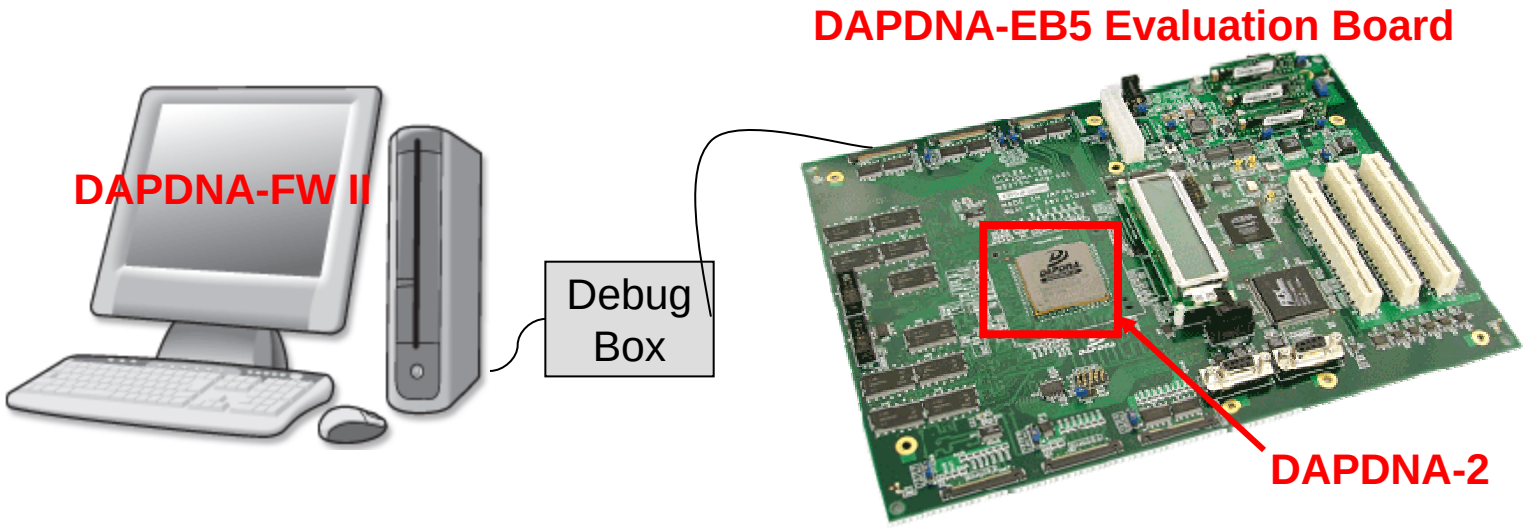
- **Programming Example and Performance**

Using dynamic reconfigurability to change image filters

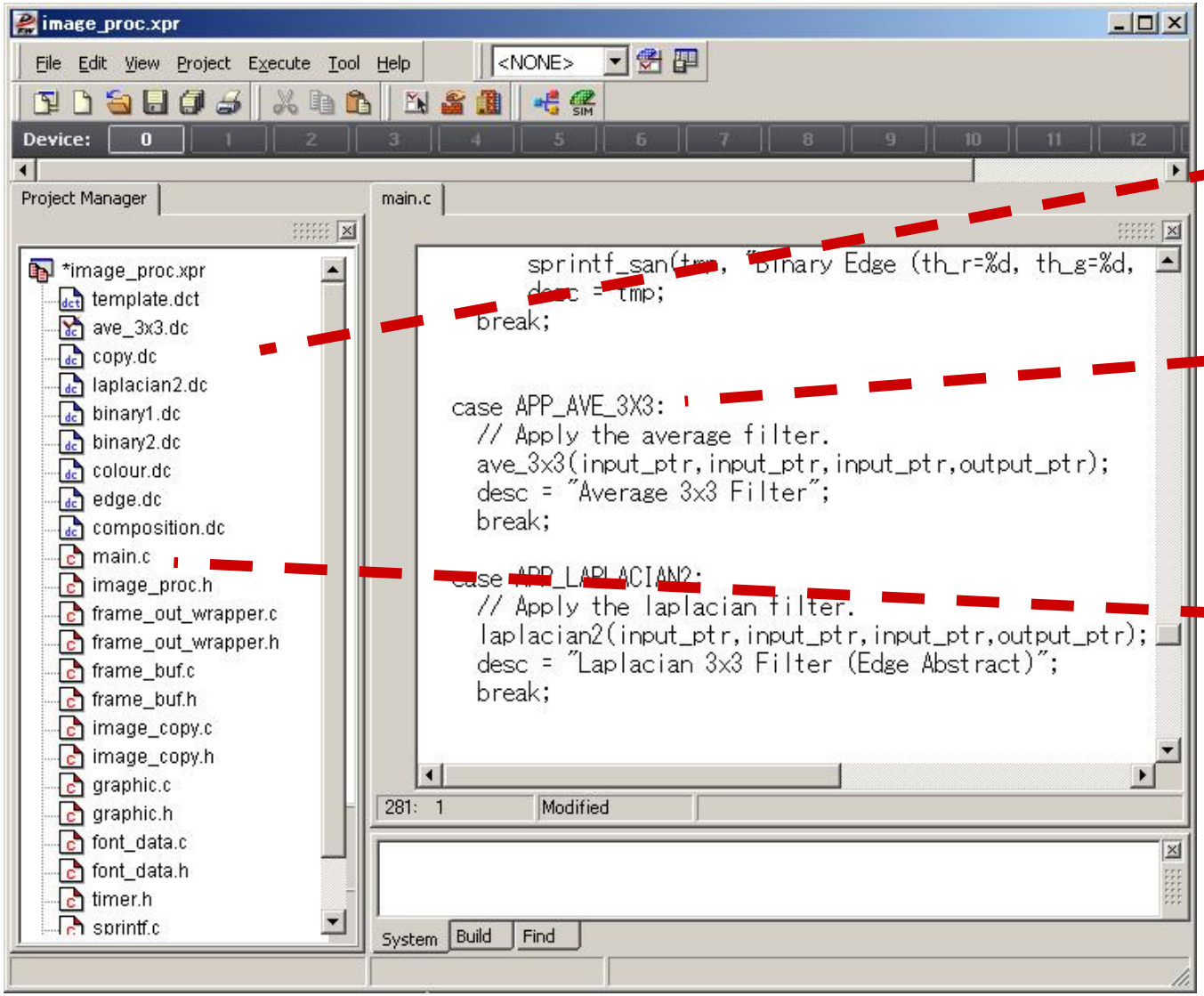


Various image filters written in DFC and compiled

- Laplacian
- Binary
- Average
- Etc.

Filters run on DAPDNA-2 using dynamic reconfigurability of hardware

DAP calls DNA configurations with simple function calls

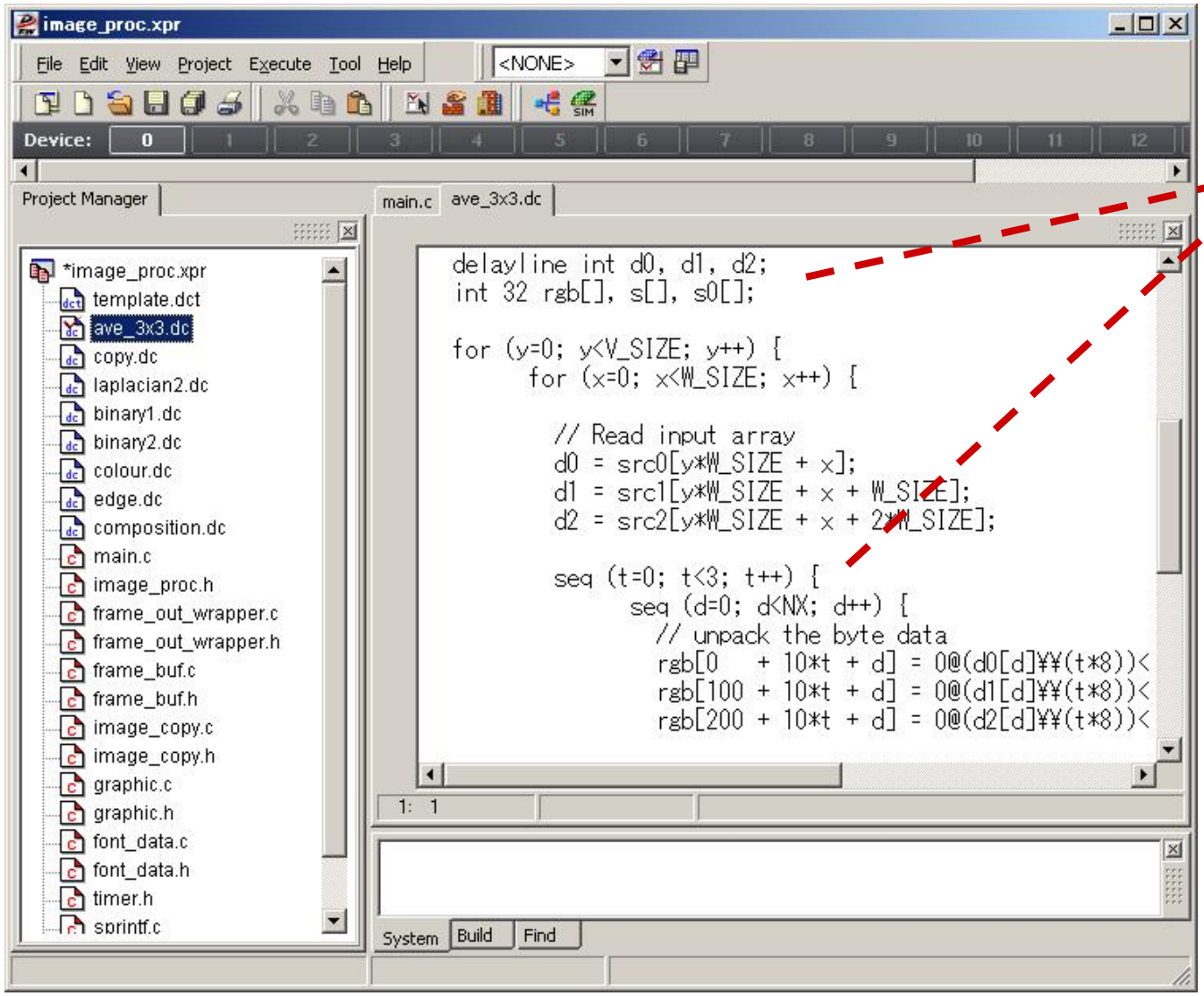


List of filters written in Data Flow c

An Average3x3 filter being called in main.c as a function

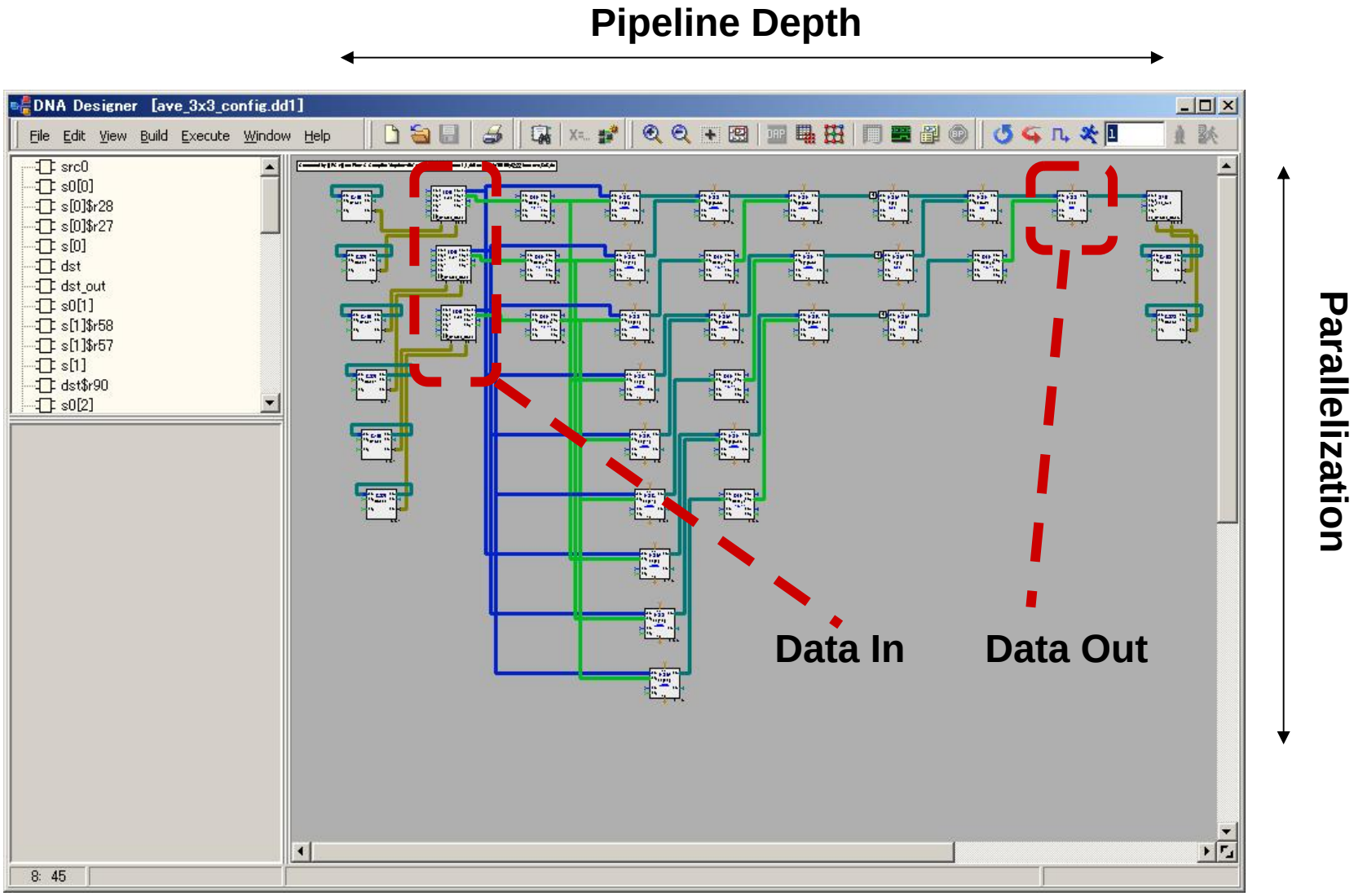
Main.c for DAP RISC

DFC-described filters compiled into HW with a single click of build button…

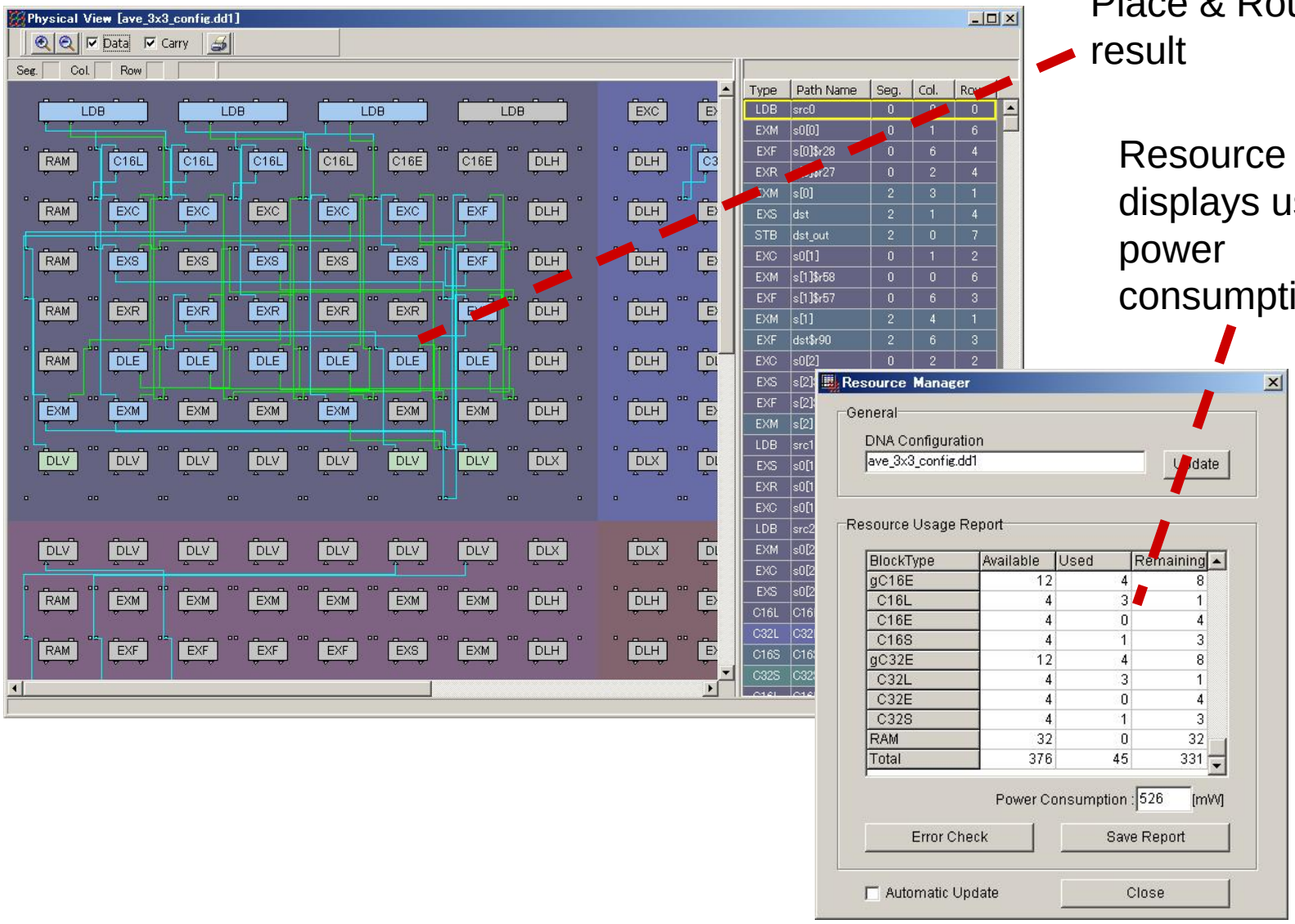


Average3x3 filter described in DFC uses delayline and seq commends to take advantage of parallelization

…resulting in a logical representation of the filter with 32-bit processing elements…



…as well as physical mapping on DNA



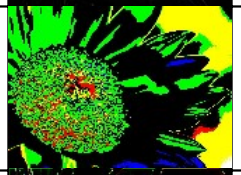
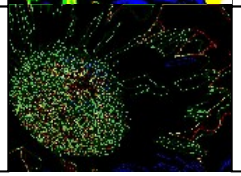
Place & Route result

Resource manager displays usage and power consumption

DFC compiler result for image filters

Image Filters		DAPDNA-2 (166 Mhz)						
		EXE	EXM	RAM	DLE	Parallel	Performance	
							M Pixel/sec	Fps(800x600)
3x3 Average	Usage %	12.5	10.7	0	5.1	3	**292**	203
Binary	Usage %	5.4	3.6	0	1.5	3	**498**	346
Binary Image Edge Det.	Usage %	5.4	3.6	6.3	1.5	1	**292**	203

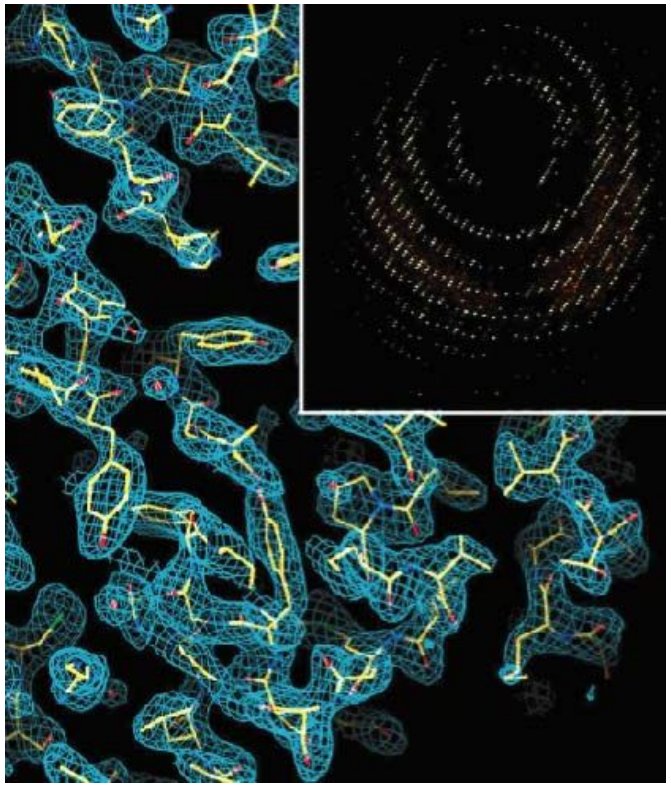
Optimized result with DNA Designer (Block Diagram) tool

Image Filters	Images	Performance (M Pixels / s)		Performance Multiple
		Pentium 4* (3.06Ghz)	DAPDNA-2 (166Mhz)	
3x3 Average		15.5	**664.0**	**43**
3x3 Laplacian (Edge Enhancement)		15.8	**664.0**	**42**
3x3 Laplacian (Edge Detection)		15.8	**664.0**	**42**
Binary		225.0	**839.0**	**4**
Binary Image Edge Detection		38.6	**664.0**	**17**

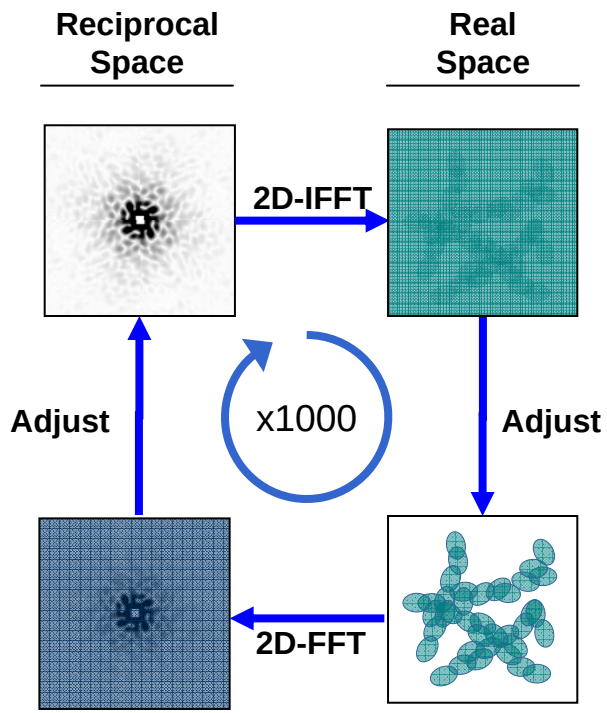
* Pentium4@3.06GHz, Red Hat Linux 8.0, gcc 3.2, SIMD instruction not used, 24bit color, 800x600 pixels, 1000 Repetitions, Average performance (pixel/sec)

FFT: Protein structure analysis

- Extrapolating molecular structure from X-ray diffraction image



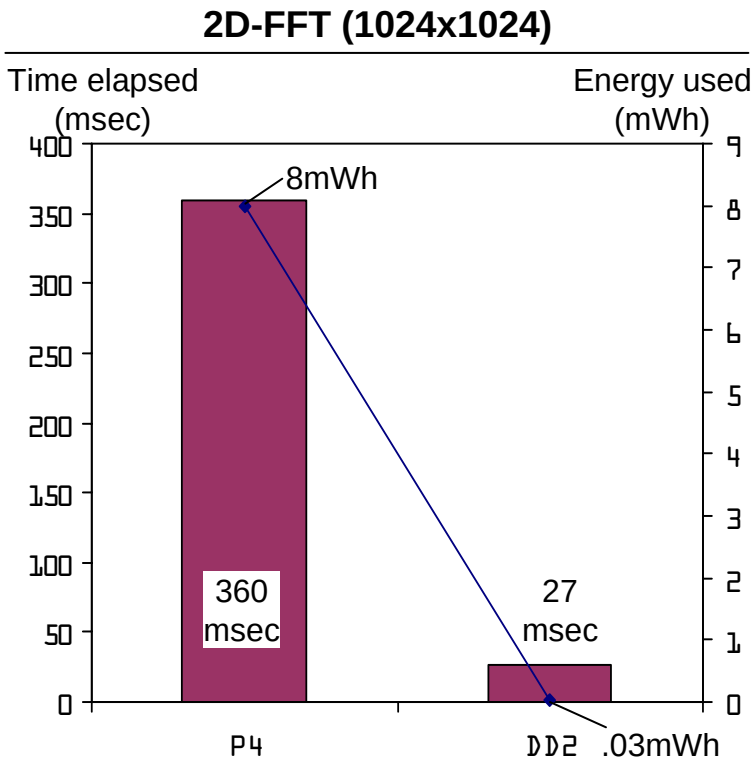
- Extrapolation Algorithm (HIO)

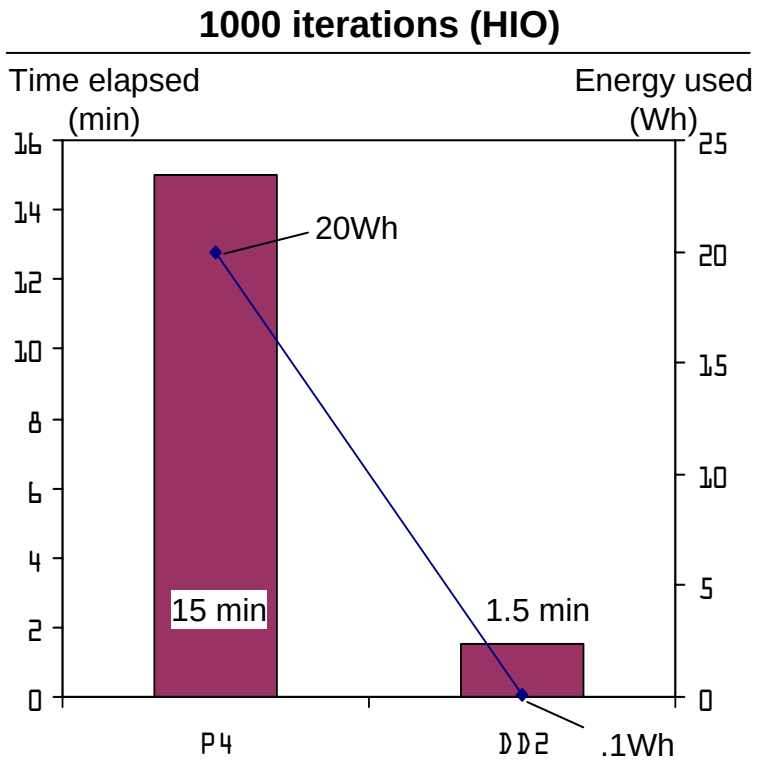


- Requires 1024 X 1024 32-bit FFTs

Source: RIKEN

DAPDNA-2 is 10X faster than P4 with 1/200 energy

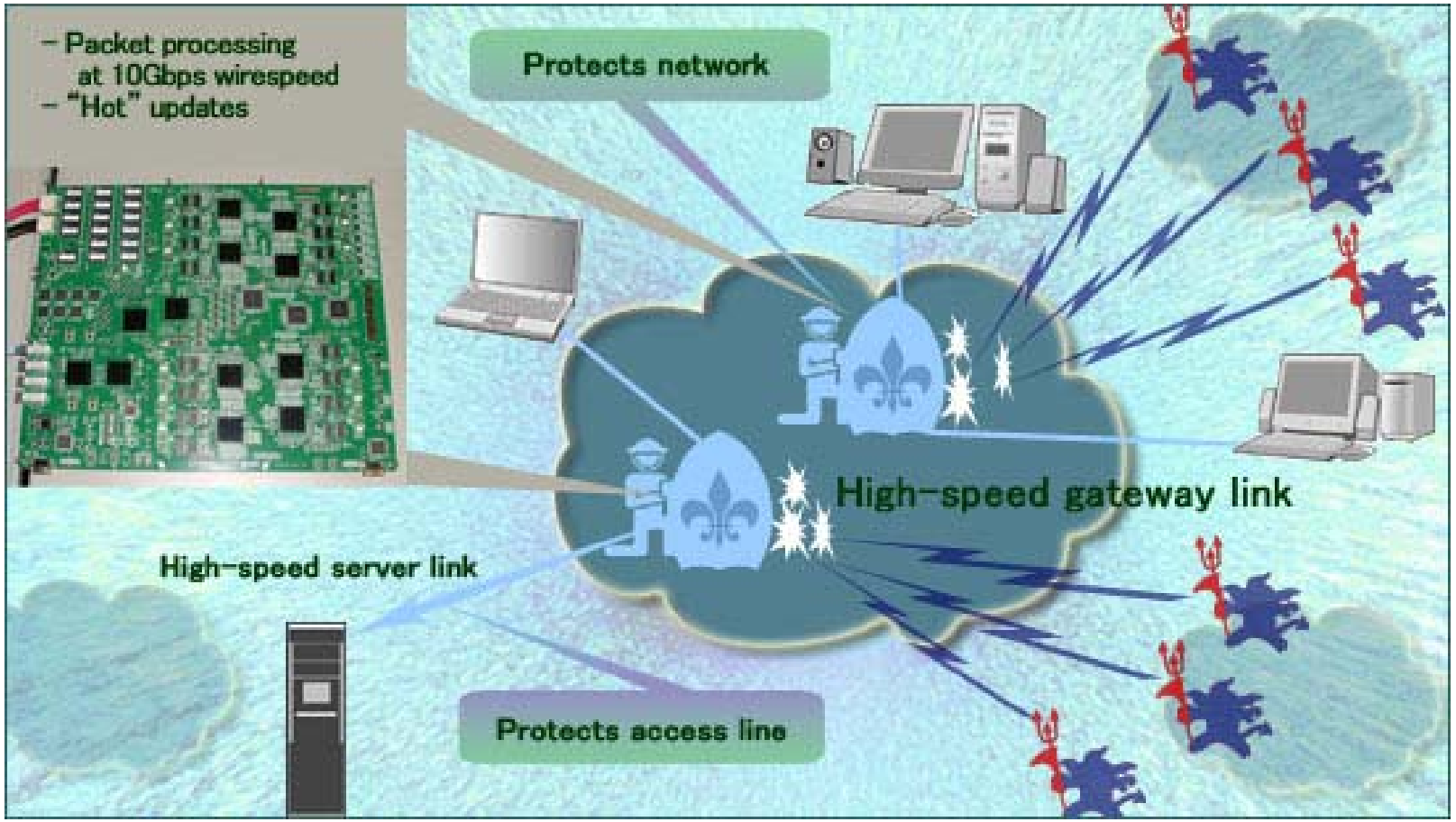




Time	13 : 1	10 : 1
Energy	267 : 1	200 : 1

* Assuming 80W for P4 and 4W for DAPDNA-2
Source: IPFlex experimentation

10Gbps active firewall by NTT



10Gb/s Firewall System using Reconfigurable Processors
Reconfigurable system technical committee

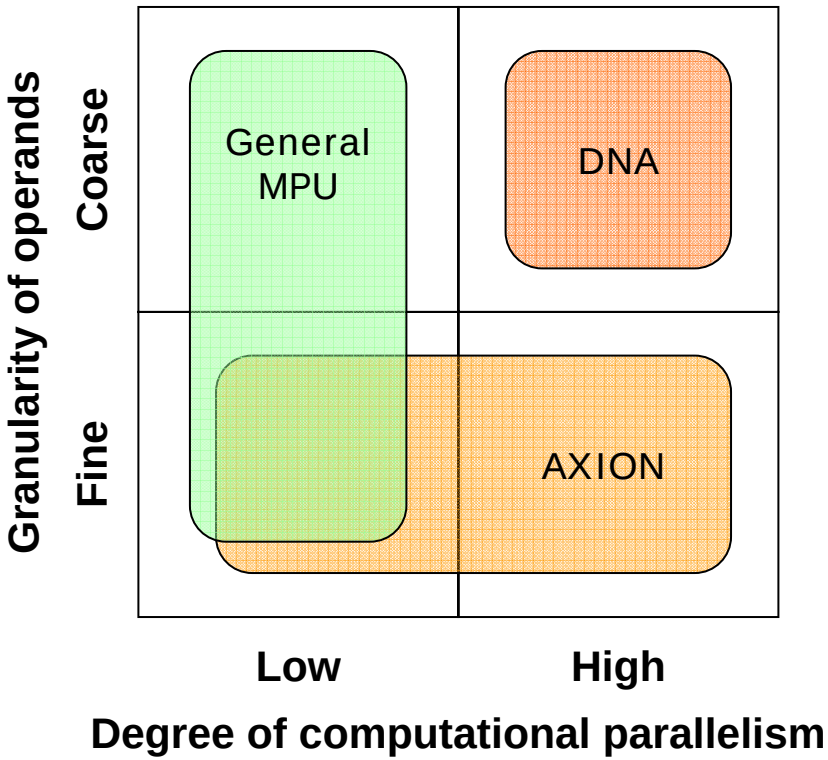
10Gbps active firewall by NTT

- **"Hot" update capability**
  - Hardware circuits can be updated without interrupting service
- **Guaranteed 10Gbps packet processing**
  - 10Gbps wire-speed is guaranteed, even with a succession of short packets
- **L4 flow classification**
  - Various flow classifications supported, including inside and outside of Netmask

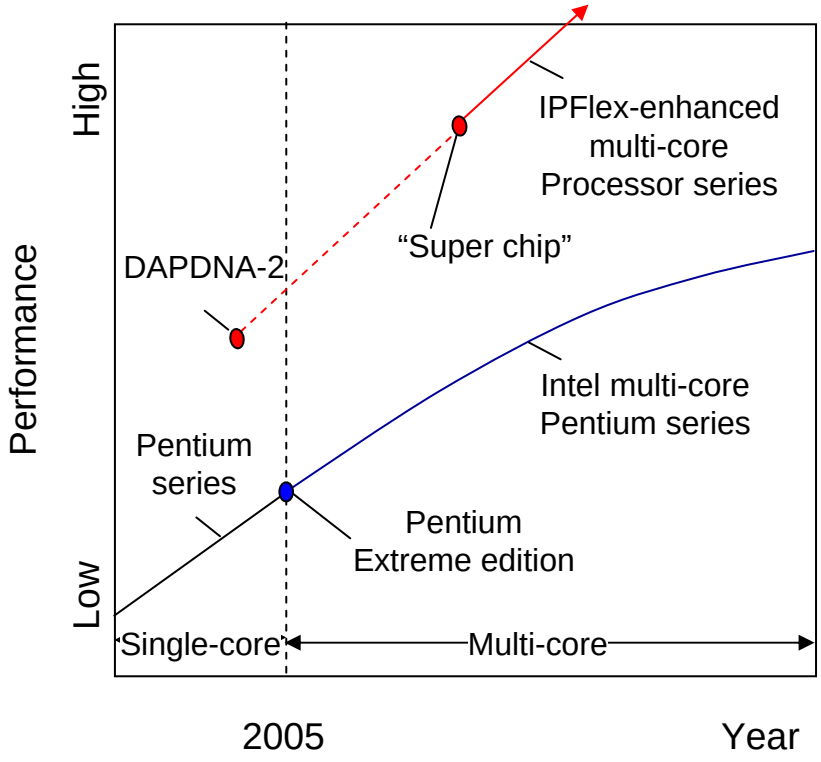
10Gb/s Firewall System using Reconfigurable Processors
Reconfigurable system technical committee

IPFlex's technology / product roadmap

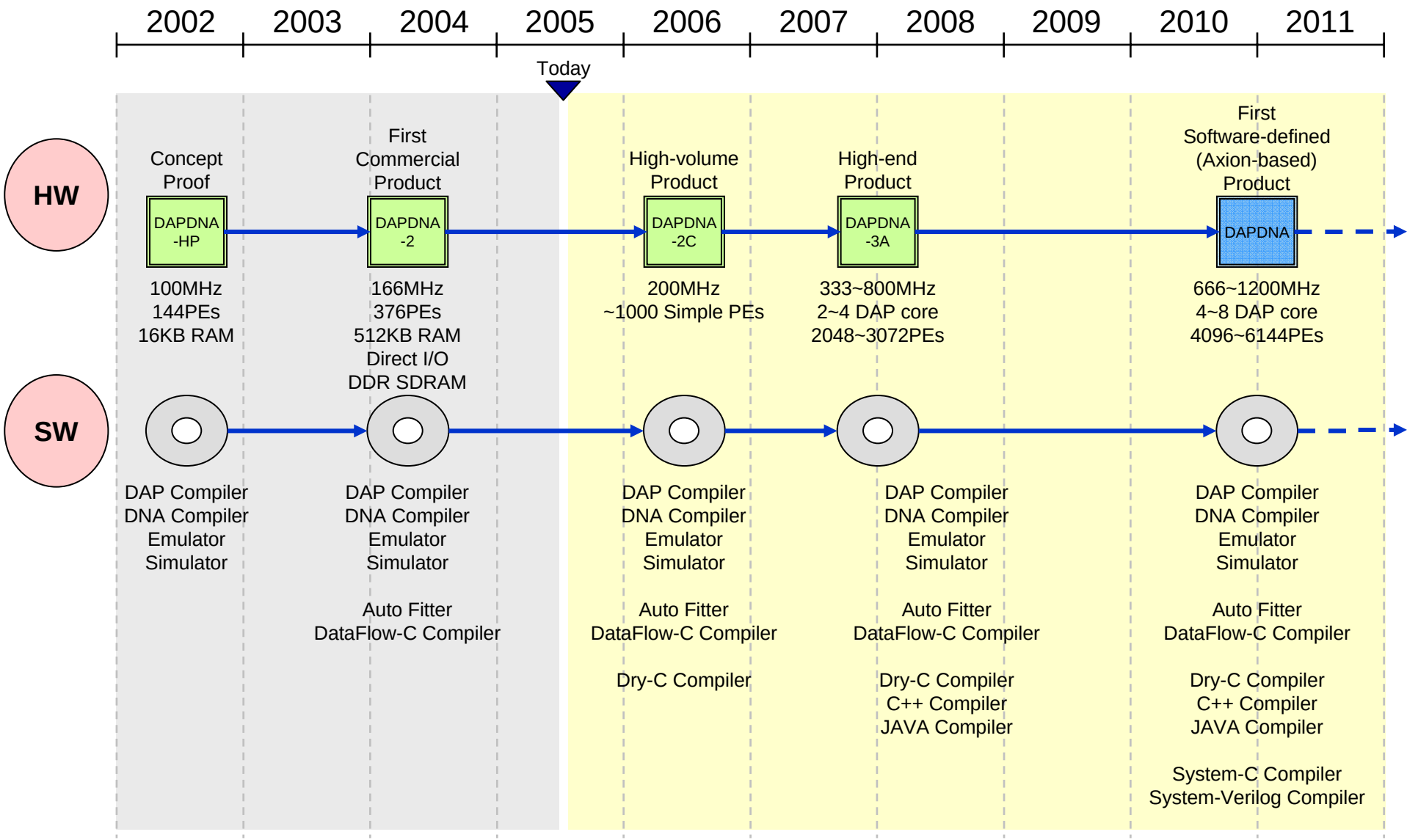
General MPU like Pentium and DNA+AXION complement well



Realizes extreme performance



IPFlex's technology / product roadmap



Dynamically Reconfigurable Processor
and
C-Based Hardware Design Platform

by

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