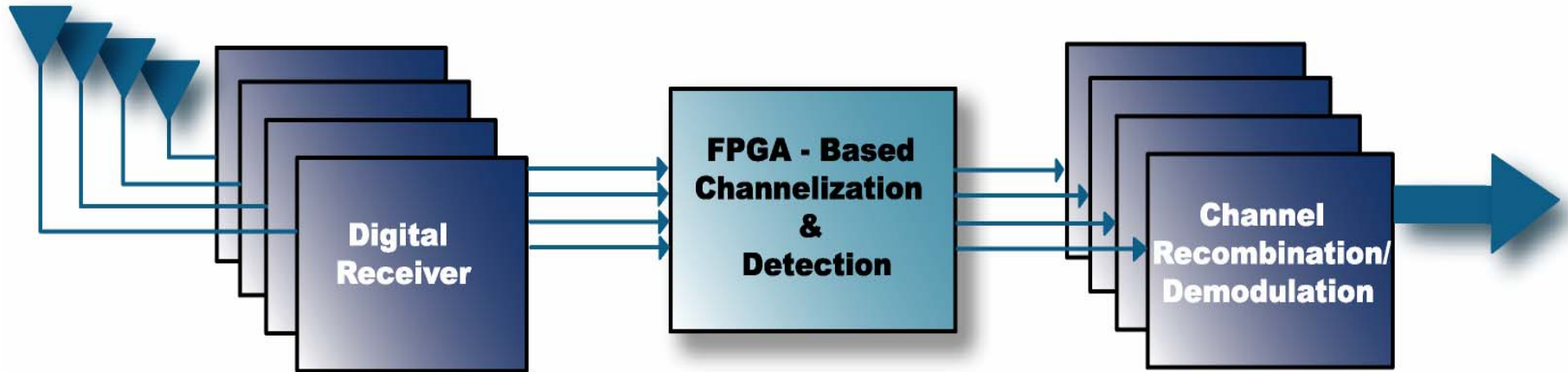


FPGA Based Signal Acquisition System

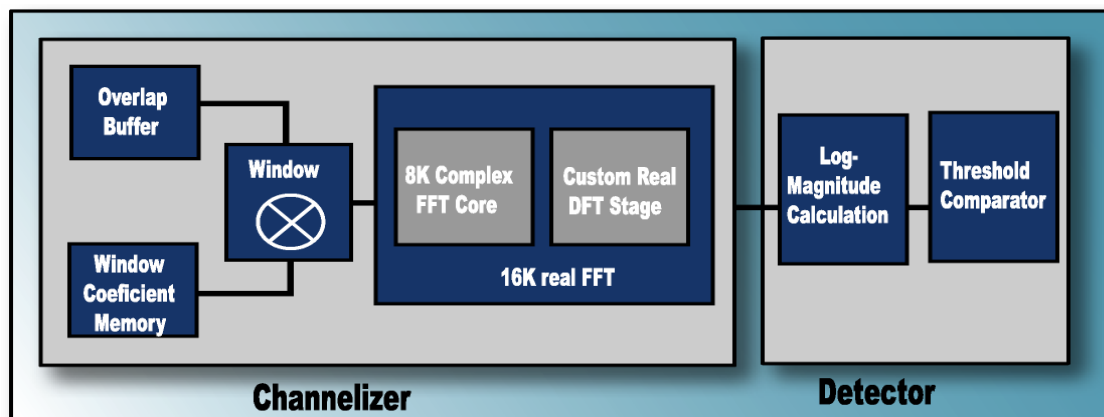
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- **Objective** : Develop a FPGA based real-time 4 channel signal acquisition system composed of frequency channelizers and signal detectors in a single 6U VME slot



- **Motivation** :
 - Benchmark computational density between FPGAs & PPCs for a typical streaming application
 - Analyze FPGA integration into a heterogeneous computing environment
 - Examine interoperability of COTS components due to emerging I/O standards such as VITA 49 (Digital IF)

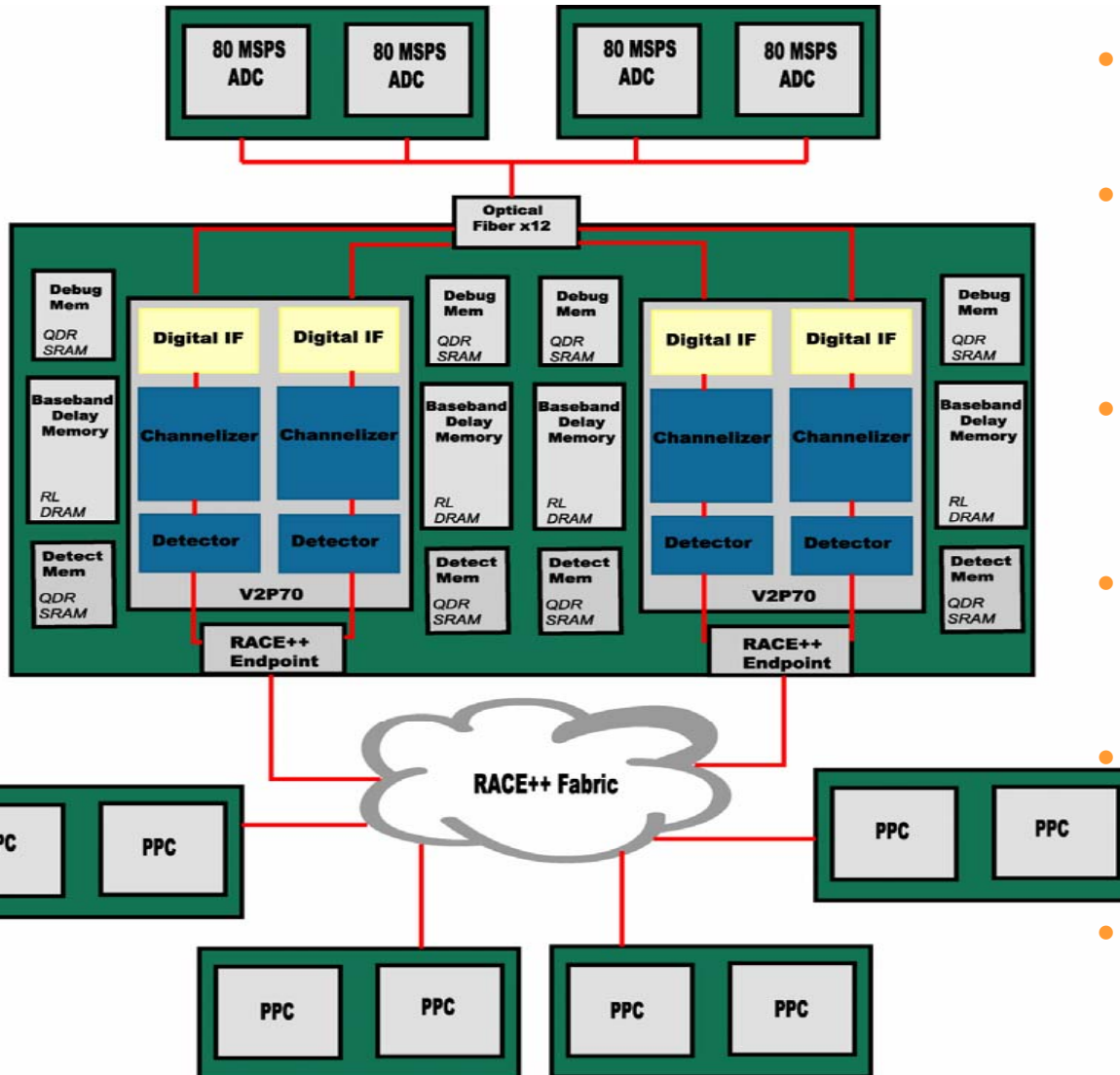
- The signal acquisition system separates a wide radio frequency band into a set of narrow frequency bands to enable automatic detection and exploitation of signals of interest
- Processing for each incoming antenna channel is composed of a channelizer and an energy detector



- **Implementation Specifications**

- 4:1 Overlap Buffer: 16K sample buffer (Dual Ported BRAMs)
- Window Coef Memory: 8K symmetric coefficients (Dual Ported BRAMs)
- Blackman Window (Embedded Multipliers)
- 16K real FFT: 8K complex FFT (Xilinx's streaming Radix-2) with the last DIT stage implemented using custom logic
- Log-magnitude: magnitude squared computed and inputted into log table
- Threshold: adjustable register and comparator to determine detections

High performance heterogeneous systems require sophisticated I/O solutions



- Data streams into the FPGA in Digital IF packets over fiber links running at 2.5 Gbps
- VITA 49 prototype cores in each V2P70 device parse packets
- Each input is channelized; baseband data is stored in delay memory and passed to the energy detector
- In the detector the log-magnitude of the data is calculated and compared to the threshold value
- Frequency bins that exceed threshold are stored in detection packets in memory
- The FPGA DMA's detections to downstream PPCs for clustering across time and frequency
- PPCs determine signals of interest and DMA baseband data from delay memory for channel recombination and demodulation