VSIPL++
A Signal Processing Library
Scaling with Moore's Law

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Hardware Trends

Greater Parallelism

- Multiple Cores
- Tiles
- SIMD

Greater Complexity

- Memory Hierarchy
- Scheduling
- Interconnect

Polymorphism

Greater Integration

VSIPL++

Blocks

- Logical View of Data
- Extensible

Maps

- Parallelism
- Physical Layout of Data

Early Binding

- Analyze Processing

Expression Templates

- Domain Optimizations
- Compiler Front-end

High-Level Design