FPGA-Based Signal Acquisition System

Sarah Leeper (sleeper@mc.com), Robert Frisch (bfrisch@mc.com),
Scott Geaghan (sgeaghan@mc.com), Scott Tetreault (stetreault@mc.com),
Mike Vinskus (mvinskus@mc.com), Erich Whitney (ewhitney@mc.com)
Mercury Computer Systems, Inc., Chelmsford MA 01824

Abstract

This paper presents a high-performance four-channel signal acquisition system composed of frequency channelizers and signal detectors in a single 6U VME slot. The intense computational complexity necessary to implement such an application requires field programmable gate arrays (FPGAs) to achieve a 10x performance density increase over a traditional GPP implementation. The same application performed on a G4 platform utilized 10 processors, thus indicating a significant savings in size, weight, and power by using FPGA technology.The signal acquisition system was implemented using a RACE++-based FPGA board equipped with two Virtex-II Pro 70 devices and an FPGA Development Kit (FDK) to provide infrastructure components that reduce development time, thus facilitating time to market and mitigating possible FPGA integration risks into a heterogeneous multi-computer environment.

Specifically this paper will address the I/O concerns associated with integrating an FPGA solution into a deployable system through the use of VITA 49 over optical fiber and a buffer queue methodology to efficiently coordinate DMA transfers over the RACE++ fabric to downstream processors to take full advantage of the throughput capabilities of the FPGA platform. Additionally, we will examine the design techniques employed to implement a real-time embedded application on commercial off-the-shelf (COTS) hardware.

Introduction

Each of the four antenna channels comprised in this FPGA- based signal acquisition system can be divided into two functional parts: the channelizer and the energy detector. The purpose of a channelizer is to separate a wide radio frequency band into a set of narrow frequency bands to enable automatic detection and exploitation of radio frequency signals of interest. To identify such signals, the channelizer is typically paired with a detection mechanism that flags changes in energy emittence. The detection events are then encoded with the time stamp, the frequency bin number, and the quantized log-magnitude representation of the channelized data. Further downstream PowerPC (PPC) processing identifies the signals of interest, via a clustering algorithm, and requests the FPGA for specific baseband data for demodulation.

Architecture Overview

Figure 1 depicts our four-channel system architecture. One V2P70 FPGA is responsible for the channelization and detection of two independent antenna channels. Each channel receives 14-bit ADC data at 80 MSPS over optical fiber using Serial FPDP (VITA 17.1) and Digital IF protocol (VITA 49). The streaming data is then processed in real-time through the channelizer and detector IP blocks at an internal processing clock of 175 MHz, thus achieving about 12 GOPS, or 48 GOPs per slot. The resulting detection packets are stored in QDR SRAM to be DMA'd using Buffer Queues from the system board to up to eight PPCs per channel for cluster processing. Once the PPCs determine the signals of interest, a request is made to retrieve the basebanded data from RLDRAM. The DSP IP, as well as the supporting infrastructure for a single channel signal acquisition system, requires 39% of the chip's slices and 31% of the BRAMs.

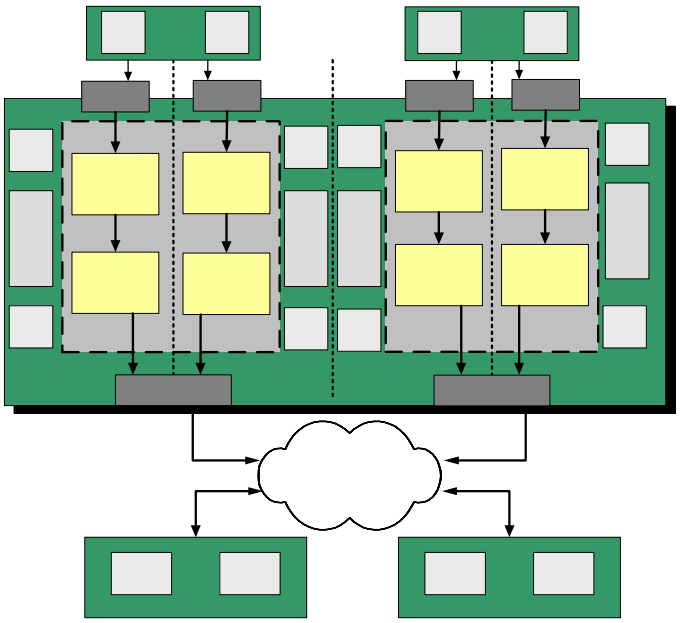

Figure 1 : Four-channel signal acquisition system architecture.

The channelization technique employed by this application is an FFT-based weighted overlap method, where a block of 16 K samples are buffered, multiplied by a Blackman window, and then transformed to the frequency domain. To reduce aliasing in the narrowband

channels a 4:1 overlap was used, therefore inflicting a 4X increase of the processing rate over the input rate. To accommodate such a requirement with minimal impact on FPGA resource utilization, a combination of algorithmic modification and increased processing rate was used. Because the 16K input block is a real-valued sequence, a Xilinx CoreGen 8K complex radix-2 FFT could be used with the final DIT stage implemented independently. This coupled with doubling the processing rate (minimally 160 MHz) enables only a single instance of the FFT to be realized while maintaining real-time input data rates.

Detection processing involves the taking of the log-magnitude of the channelized data and comparing it to a predetermined yet adjustable threshold value. If the data sample exceeds threshold it and its frequency bin number are stored in a detection packet to be off-loaded from the FPGA. Figure 2 depicts the dataflow of the IP.

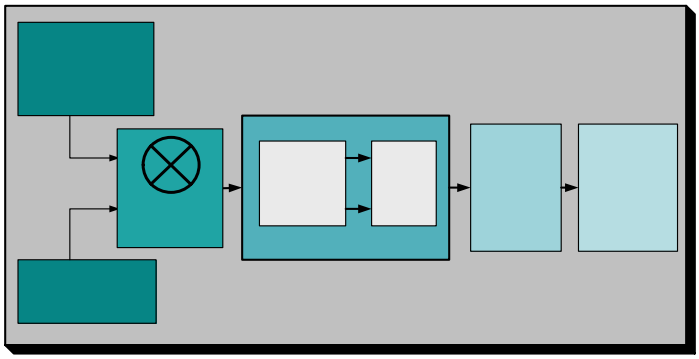

Figure 2 : Signal acquisition processing flow.

I/O Considerations

Characteristically, FPGA applications are computationally dense, and exploit the streaming nature and inherent parallelism in typical DSP algorithms. While the technology can handle these rigorous computations internally, it is often the I/O bandwidth and format that constrain the platform. The implementation of this application highlights the use of two different I/O methods, streaming sensor and block-based DMA over high-speed switch fabric that are enabled by the FDK environment.

VITA 49 (Digital IF)

High-speed digitized data transfer from receiver to signal processor elements such as FPGAs, is a common requirement in today's military systems. Implementation of non-standard interfacing solutions can lead to interoperability issues that can result in delays in time to market and costly IP module redesigns. VITA 49 is a current effort to standardize this transfer of high-speed digitized intermediate frequency (IF) output from tuner/receiver channels to computer elements. This protocol provides a packetized structure that offers a flexible header format coupled with the data payload. This application uses a prototype version of this standard that can achieve a transfer rate of 250 MB/s over optical fiber, to handle the data formatting from the ADC. In this instance the VITA 49 protocol is built upon a Serial FPDP (17.1) link layer enabled by Xilinx's RocketIO technology. This use of such a protocol provides a deterministic communication interface that promotes interoperability between COTS vendors.

RACE-On-Chip and Buffer Queues

Another necessary I/O aspect of most FPGA applications is the communication across the backplane to other compute elements. The FDK provides a unique and efficient methodology by extending the RACE++ switch fabric on to the FPGA itself. This way each memory or IP component connected to RACE-On-Chip (RoC) can be accessed by any other processor within the system, thus providing scalability and seamless integration of FPGA solutions into large-scale systems. Furthermore, RoC along with FDK's DMA engine allows the FPGA to master DMA transfers to the rest of the multicomputer. This ability is key to maximizing FPGA efficiency, since the FPGA is capable of extremely high throughput. FDK has extended this concept to include the ability to DMA data produced by the FPGA to multiple downstream compute elements through the use of buffer queues. These modules are able to facilitate multi-node communication through simple MCOE dx API calls.

Conclusions

FPGAs are an integral part of the heterogeneous processing environment typical in military applications. As shown with this four-channel signal acquisition system, highly parallel streaming DSP applications are a good fit for this platform and with the advent of better I/O technologies and standards, the risk of integration into large deployable systems is greatly mitigated. Additionally, the availability of such FPGA development kits provide the infrastructure necessary to enable FPGA designers to focus on developing the application itself and successfully deploy their systems in a timely fashion.

References

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