Implementation of an Embedded DoD VSIPL Application on the DARPA Polymorphous Computing Architectures (PCA) RAW Processor

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This briefing describes an effort to implement an advanced embedded DoD signal processing algorithm on a Polymorphous Computing Architecture (PCA), under development by DARPA, using the VSIPL industry standard signal processing API. Critical embedded, high performance radar processing algorithms for shipboard ballistic missile defense have been implemented at Lockheed Martin MS2 in COTS PowerPC architectures using equipment from various vendors, including CSPI, Mercury Computers and Sky Computers, utilizing standard API libraries such as VSIPL and MPI. Of particular interest is how can we easily port these embedded applications from conventional COTS architectures for execution on embedded PCA morphable processor architectures? The goals of this effort were to:

- Demonstrate a critical embedded DoD signal processing benchmark using an industry standard API (VSIPL) executing on a DARPA Polymorphous Computing Architecture (PCA RAW)
- Compare the software environment, performance, size, power and cost with existing embedded COTS PowerPC-based processor static architectures with a PCA morphable architecture
- Evaluate the potential use of industry standard APIs and Portability Standards, such as VSIPL, MPI and DRI, in a PCA computing environment
- Demonstrate the key embedded PCA technology, running a DoD Benchmark written in VSIPL, for key US Defense Department representatives and develop a concept to transition PCA-based architectures into embedded DoD tactical systems

This new technology, being developed by the DARPA Polymorphous Computing Architectures (PCA) Program, promises to provide an alternative, morphable embedded computing architecture as compared to classical, static PowerPC or Pentium-based architectures. The PCA architectures can adapt their structure by morphing their architecture as the mission and processing requirements change, thereby enhancing performance as the mission dictates architecture changes, or morphs. The PCA embedded processor designs promise to save significant equipment space and to provide a lower cost solution by providing an architecture that can adapt to the mission at hand. The issue that arises is the potential complication of efficiently programming a new, unconventional processor architecture. DoD contractors cannot afford to hire specialized architects and programmers that are adept at programming niche architectures. By providing industry standard APIs, such as VSIPL and MPI, for new PCA architectures, we hope to be able to realize legacy applications implemented in new, morphable embedded PCA hardware and middleware architectures with standard C and C++ programming techniques.

In this briefing, we describe an embedded processing application that includes Pulse Compression radar signal processing followed by an architecture morph and track processing. Processing functions are coded using a high level language (C or C++) and industry standard APIs (VSIPL and MPI) on a host processor which executes the function on an embedded PCA architecture (in this case, the MIT RAW processor). Benchmark results will be provided that compare the same VSIPL benchmark algorithm on both a conventional, static embedded architecture (such as PowerPC) and PCA-type morphable architecture (such as RAW). Finally, the results of the benchmark algorithm run on an actual PCA RAW processor, using VSIPL, will be presented.