

Panel Session:
Will Software Save Moore's Law?

James C. Anderson
MIT Lincoln Laboratory

HPEC05
Wednesday, 21 September 2005

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Panel members & audience may hold diverse, evolving opinions

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 - 1620-1650: panelist presentations**
 - 1650-1720: open forum**
 - 1720-1730: conclusions & the way ahead**



Panel Session: *Will Software Save Moore's Law?*

**Dr. James C. Anderson,
MIT Lincoln Laboratory,
Moderator**



**Dr. William Bail,
MITRE Corp.
Software Engineering Center**



**Mr. Robert Bond,
MIT Lincoln Laboratory**



**Dr. Vivek Sarkar,
IBM Research**

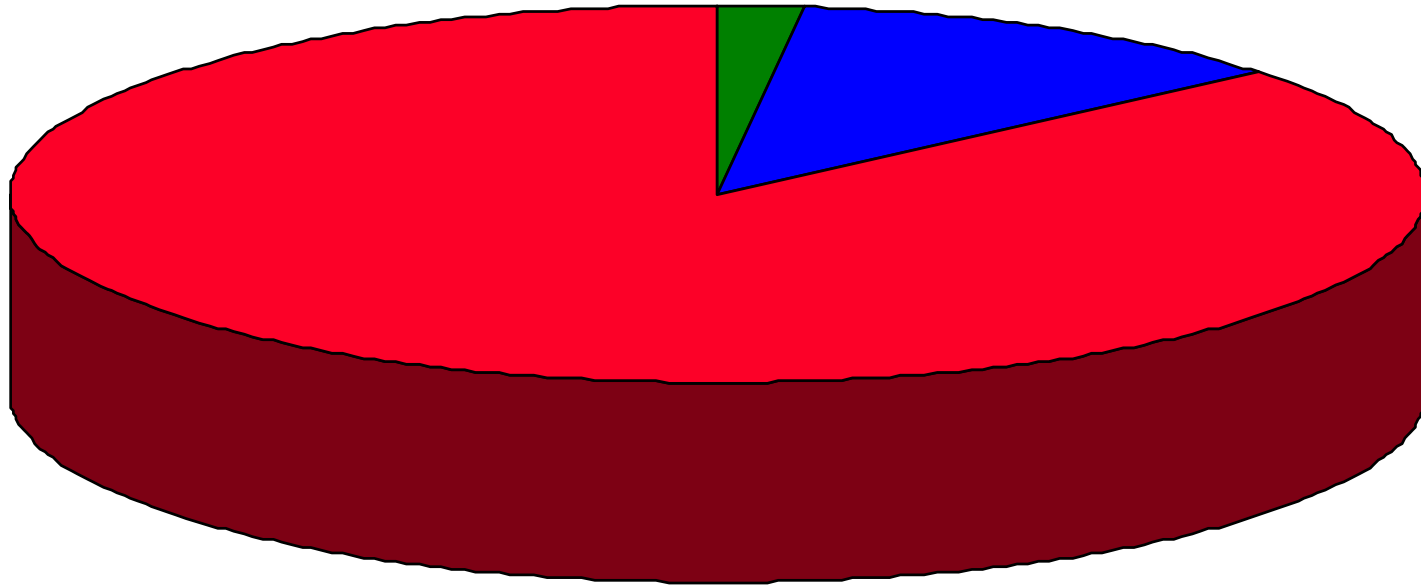


**Dr. Guy Steele,
Sun Labs**



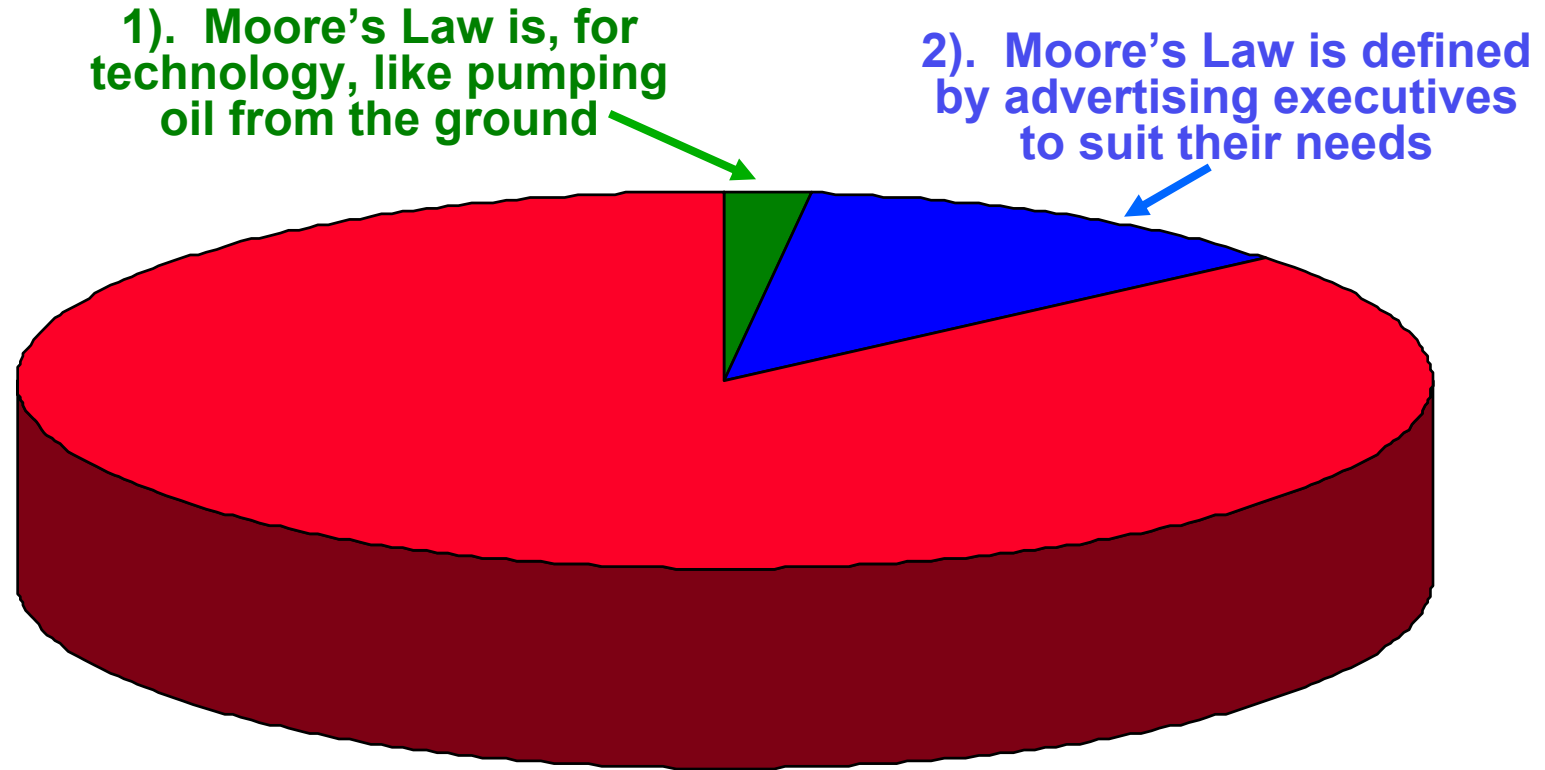
Last Year's Audience Opinion Survey

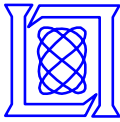
1). Moore's Law is, for technology, like pumping oil from the ground



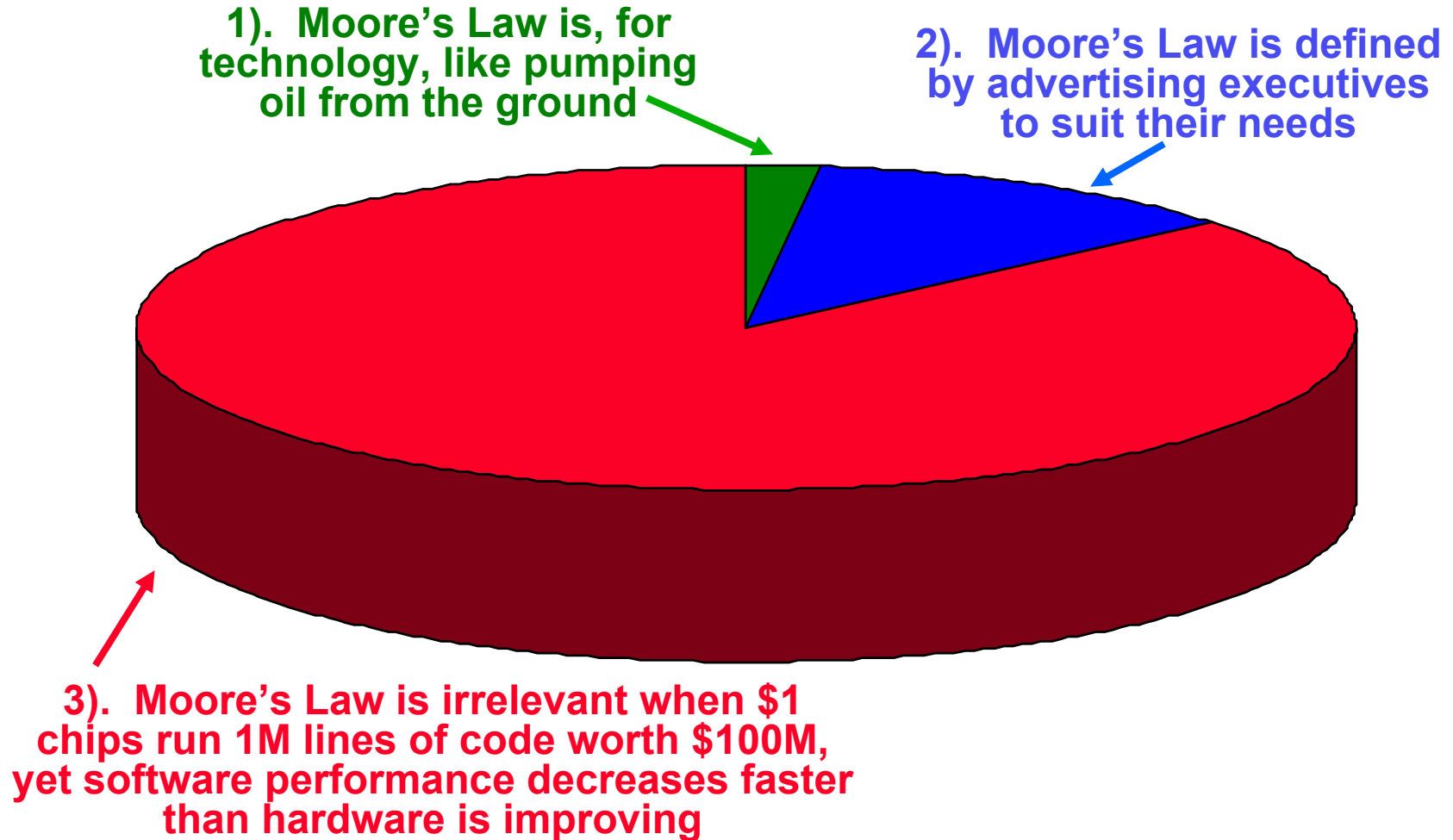


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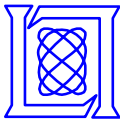
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As a result, "will software save Moore's Law?" was chosen as this year's theme



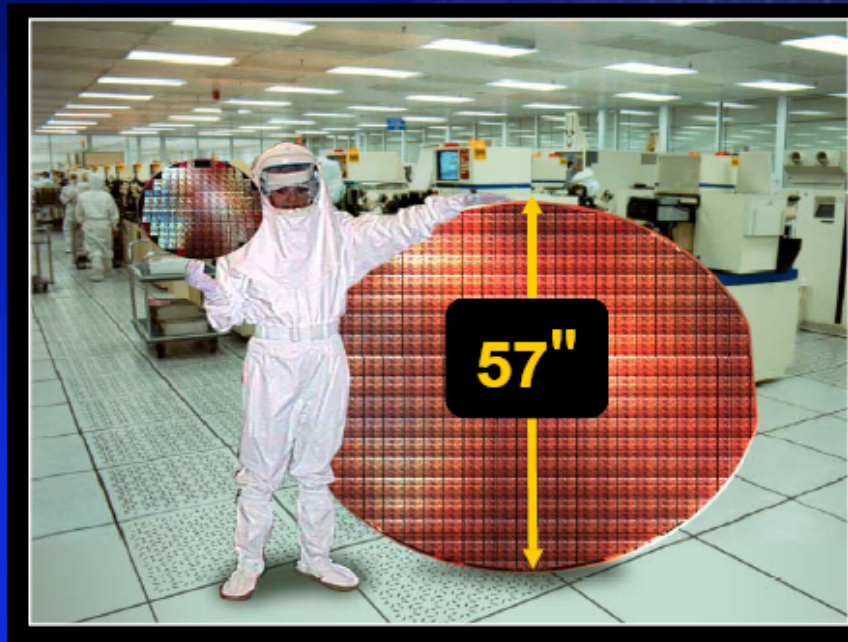
Overview



“Original” Moore’s Law (1965, revised 1975)

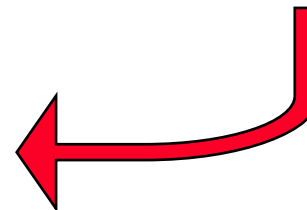
- 4X transistors/chip every 3 yrs
- Improvements came from decreasing geometry, “circuit cleverness” & increasing chip size
- Held from late '70s - late '90s for memory chips

Projected 2000 Wafer, circa 1975



Moore was not always accurate

Slide #12 from Gordon Moore’s
“*No Exponential is Forever ...
but We Can Delay ‘Forever’*,”
ISSCC03, [www.intel.com/
technology/silicon/mooreslaw](http://www.intel.com/technology/silicon/mooreslaw)





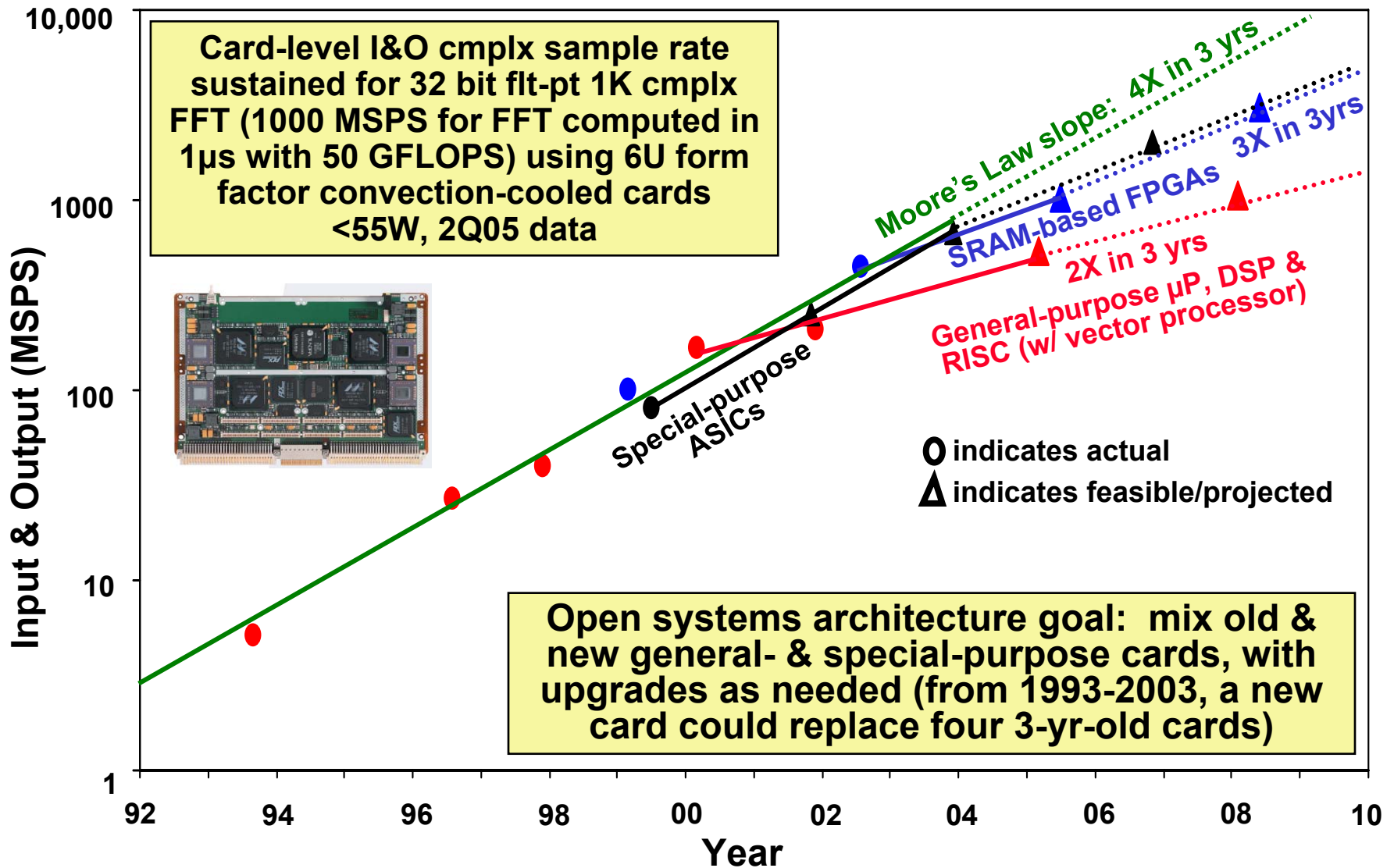
Hardware Improvement Rates Have Slowed Recently

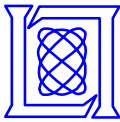
- 2004 Update of International Technology Roadmap for Semiconductors
 - Predicts future chips (through 2018) will be *same size or smaller*
 - Chip-level CMOS computing device improvements presently limited to **3X every 3 yrs** (e.g., FPGAs & ASICs)
 - 2X transistors for constant chip size every 3 yrs
 - 1.5X speed for constant power every 3 yrs
 - General-purpose microprocessors with large on-chip cache may be limited to **2X every 3 yrs**
- Improvement rates presently hampered by device-level (processor/memory) & system-level (card/backplane) I/O bottlenecks

Slower (*but still substantial*) growth rate predicted, with greatest impact on embedded systems having highest throughput & memory requirements

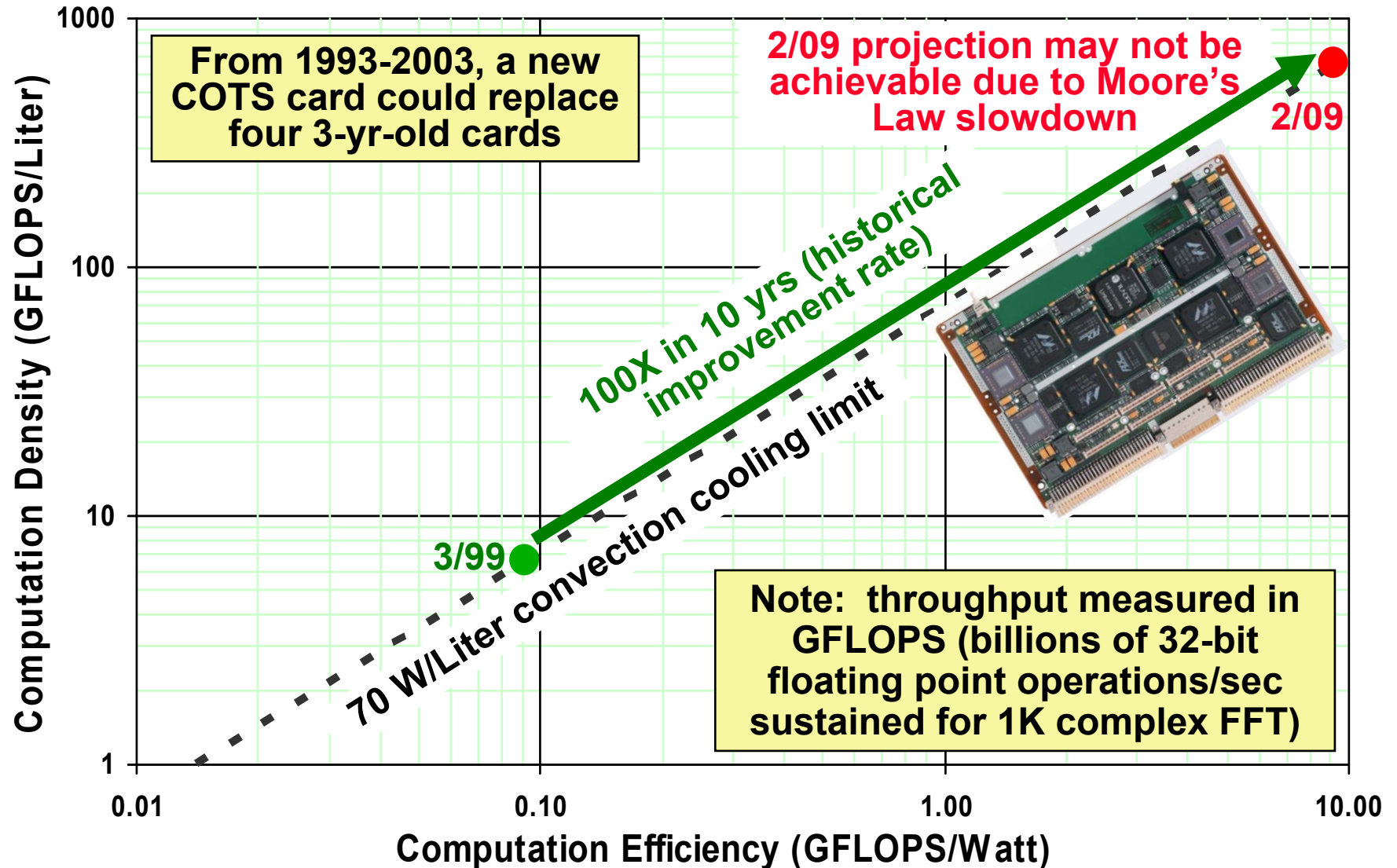


Timeline for Highest Performance COTS (commercial off-the-shelf) Multiprocessors



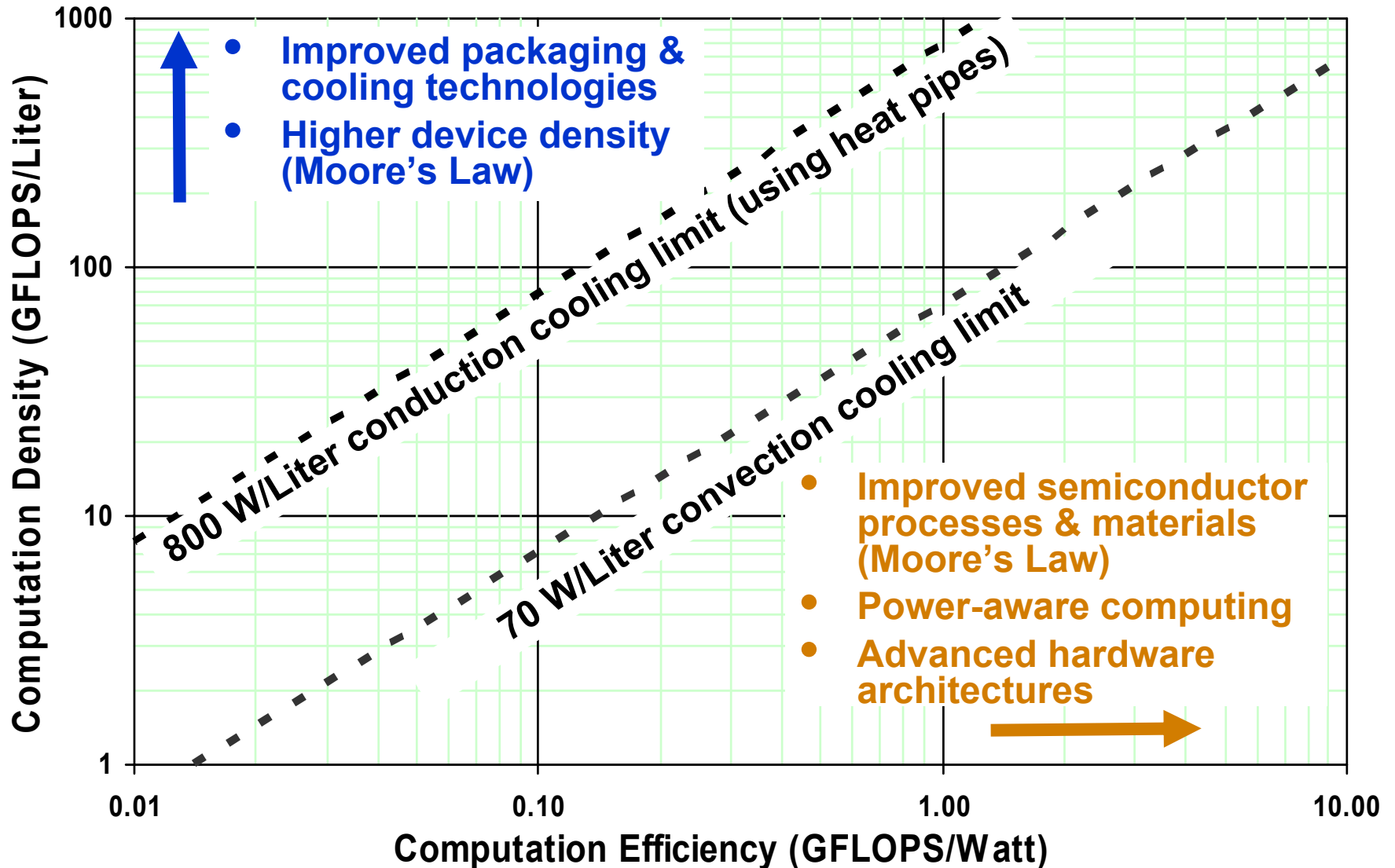


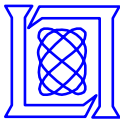
Historical Improvement Rates No Longer Apply



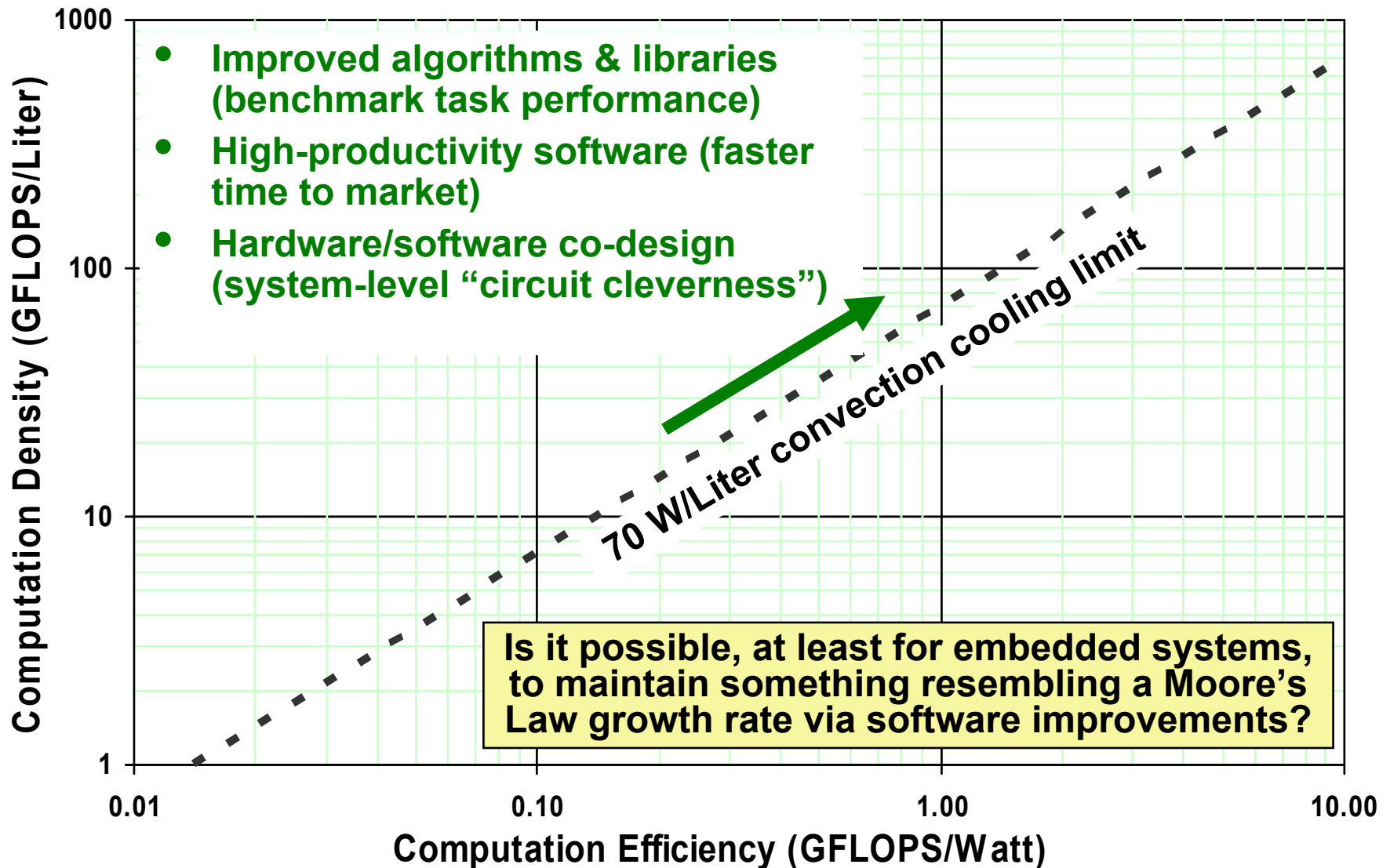


Typical System-level Figures of Merit for Embedded Processors



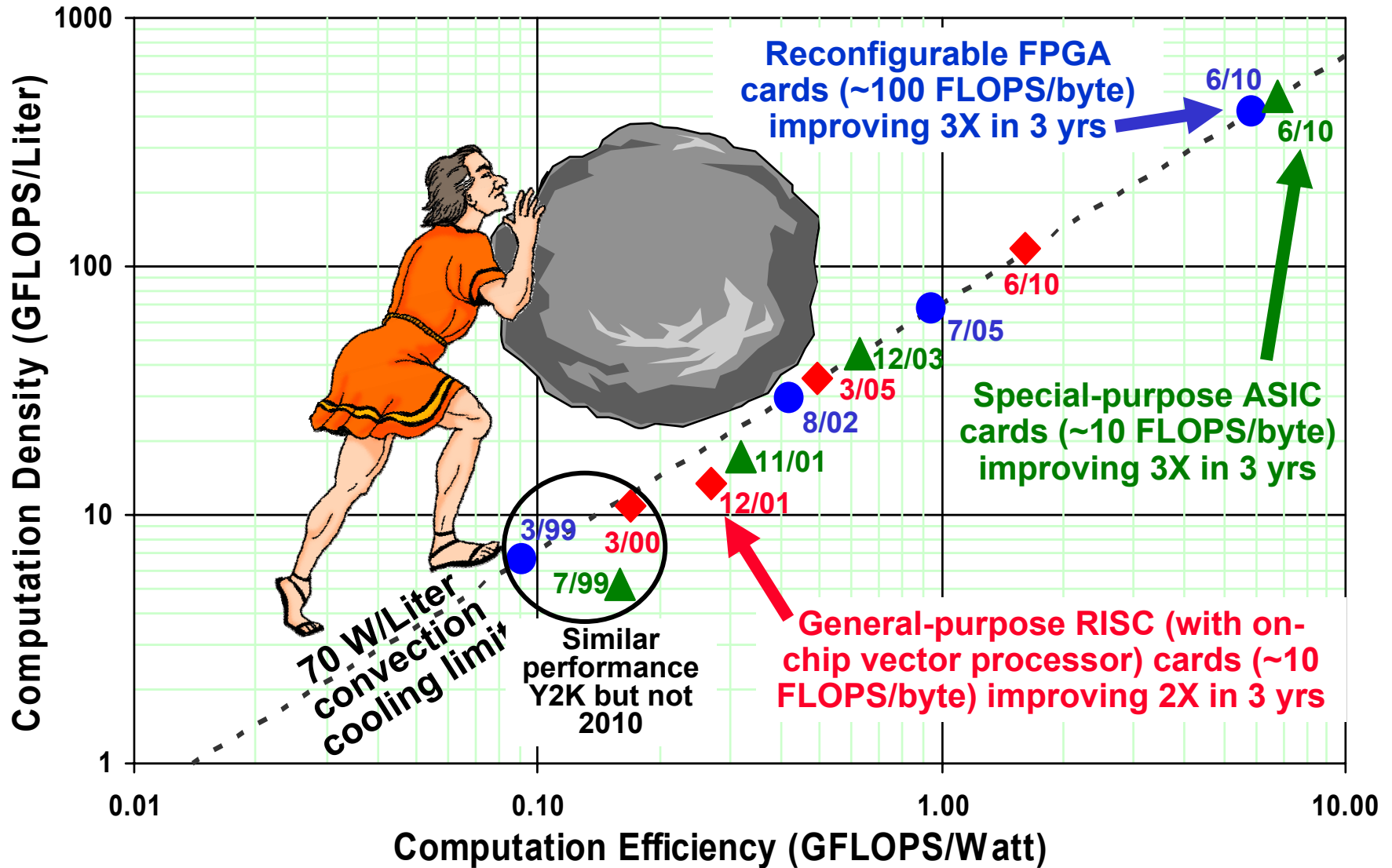


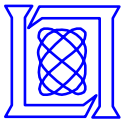
System-level Improvements From Software



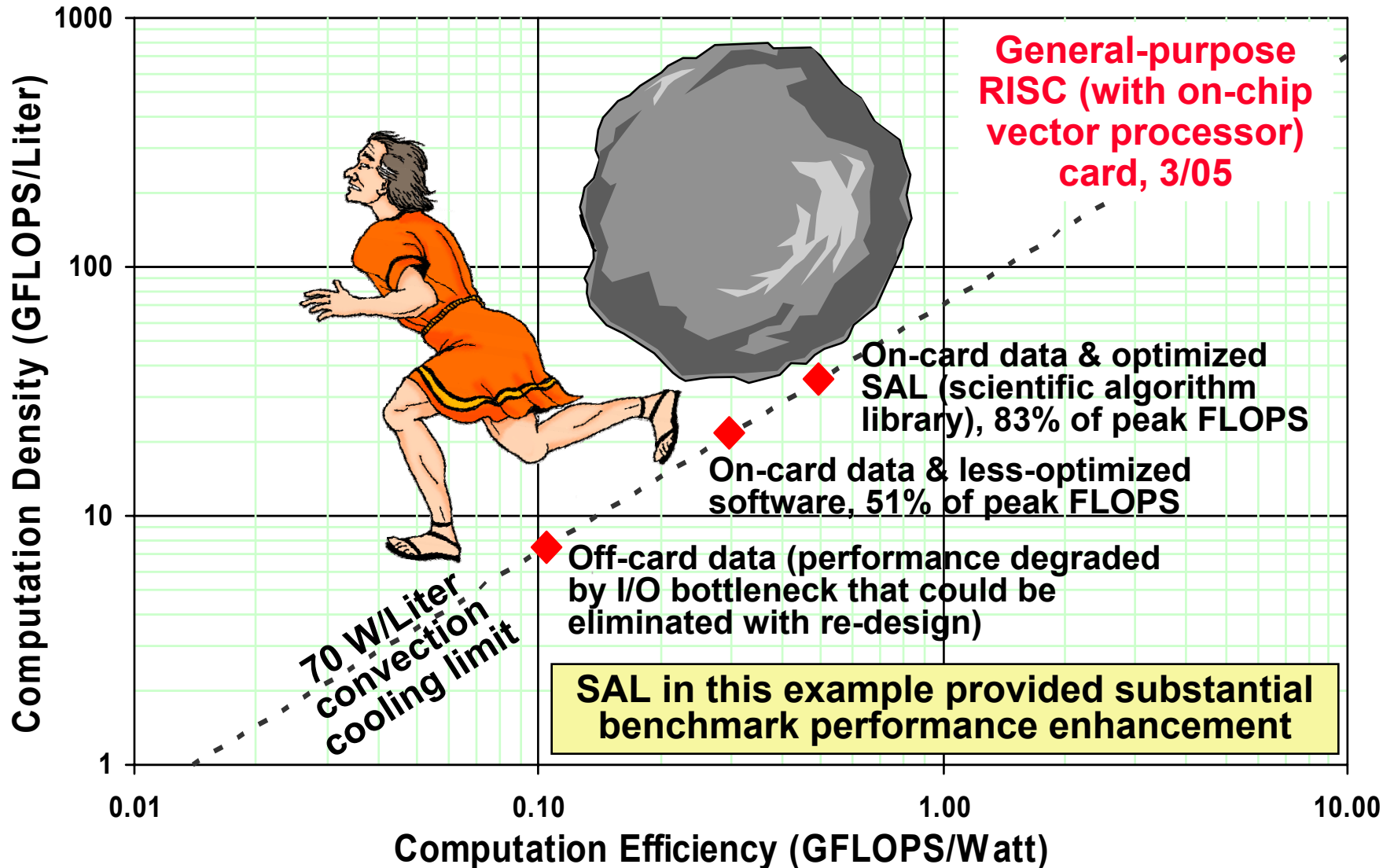


Improvements in COTS Embedded Multiprocessor Cards, 2Q05





COTS Technology Application Challenges, 3/05



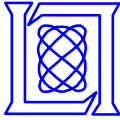


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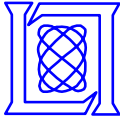


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Conclusions & The Way Ahead

- **Slowdown in Moore's Law due to a variety of factors**
 - Improvement rate was 4X in 3 yrs, now 2-3X in 3 yrs (still substantial)
 - Impact of slowdown greatest in “leading edge” embedded applications
 - COTS markets may not emerge in time to support historical levels of improvement
 - Many software issues may overshadow Moore's Law slowdown
- **Wirth's Law definitely detracts from progress, but impact might be mitigated with careful design for embedded applications**
- **High-productivity languages expected to reduce time to market, potentially contributing a speedup in product improvement rates**
- **High-productivity results may also come from automated code generation technologies**
- **Portable software remains a major challenge for many advanced platforms**

**“It's absolutely critical for the federal government to fund basic research. Moore's Law will take care of itself. But what happens after that is what I'm worried about.”
- Gordon Moore, Nov. 2001**