What Makes HPEC Applications _Challenging?_

Understanding Application/Architecture Interactions

David Koester, Ph.D.
dkoester@mitre.org

21 September 2005
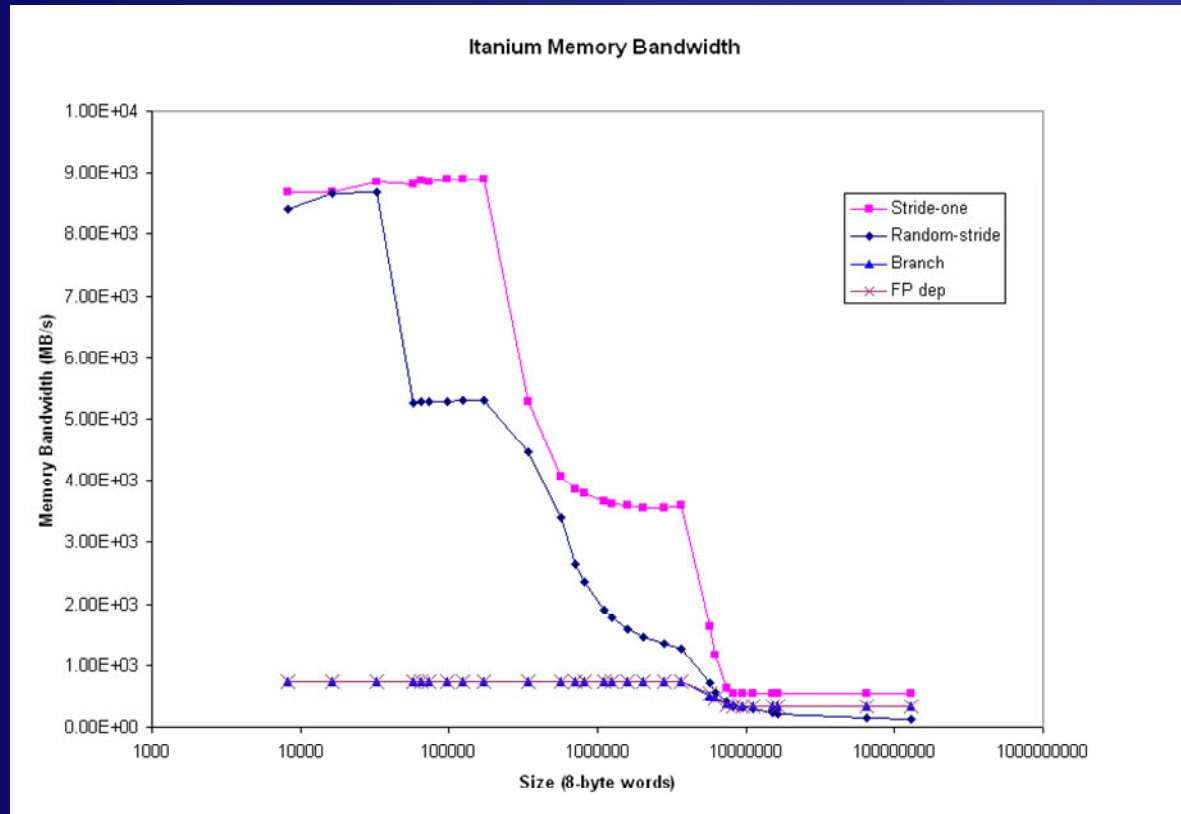
HPEC 2005
Poster Session

MITRE

Background

- **It is critical for the HEC community to be able to articulate** *"What makes HPEC applications challenging?"*
  - The *"challenging"* part has a lot to do with the *"High Performance"* in *HPE*C
    - Want to get the most out of the system
    - Go after the biggest problems
  - We must better articulate requirements to the HPEC vendor community to receive technologies that meet user needs
    - HPEC vendor community
    - HPEC research community

- *"Application Challenges"* create *"bottlenecks"*
  - The performance of a system *"in series"* is obviously limited by the lowest performance component
  - We need to apply the *"right amount"* of resources that provide the *"right"* improvement in the time to solution
    - Where is performance lost when an application is run on an HPEC architecture?
    - When does it make sense to invest in HPEC architecture to improve application performance?

MITRE

Framework addition: Data Dependency

Itanium Memory Bandwidth

PMaC Performance Modeling and Characterization Lab

San Diego Supercomputer Center

6

Branch and Data Dependencies
Intel Itanium MAPS Graph

- **Many of the issues that make HPEC applications "*challenging*" are related to the memory wall and not to Moore's Law**
  - **Minimizing the effects of the memory wall have consumed a large percentage of the transistors made available as the transistor density has increased**
  - **Degraded performance is a result of disruptions in the computational pipeline — an incidence of currency within the microprocessor**
  - **HPEC application programmers need to understand thoroughly the "*challenges*" in applications if there is any possibility for software to save Moore's Law**

1.00E+03

0.00E+00

1000   10000   100000   1000000   10000000   100000000   1000000000

Size (8-byte words)

PMaC **Performance Modeling and Characterization Lab**

San Diego Supercomputer Center

6