FPGA Implementation of MIMO Wireless Receiver in Interference

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Abstract

Multiple-input multiple-output (MIMO) wireless communication enables communication in hostile interference and multi-path environments. In this paper, a field programmable gate array (FPGA) implementation of a MIMO receiver is discussed. The MIMO system operates using two transmit and four receive antennas. The receiver implementation addresses issues of synchronization, interference mitigation, and demodulation. The implementation has two important contributions: real-time QR decomposition and back substitution for whitening input data, and adaptive beamforming. The design is specifically intended to allow for real-time detection and synchronization while in the presence of strong interference. The output of the FPGA implementation is compared to a finite precision simulation. Details of the hardware implementation are discussed.

1. Introduction on MIMO

Multiple-input multiple-output (MIMO) wireless communication provides a number of advantages over traditional single-input single-output (SISO) approaches [1,2]. One of these advantages is the reduction of the required transmit power at a given data rate because of the spatial diversity. In complicated multi-path scattering, which is common in ground-to-ground communications, the complex attenuation from each transmit antenna to each receive antenna is nearly independent to any other transmit-receive antenna pair [3]. Another advantage is the natural immunity to interference (assuming an intelligent receiver design [4,5,6]). Adaptive beamforming at the receiver can spatially mitigate the effects of interference. Furthermore, transmit diversity improves the likelihood that spatially mitigating interference does not significantly suppress power from all transmitters.

1.1 Signal Detection and Synchronization

Before the establishment of a link, the transmitter and receiver are not synchronized. To establish the link, independent known sequences are transmitted from each of the two transmit antennas. The training sequence is followed by the data sequence. The receiver recognizes the training sequence and uses it to synchronize and provide an initial weight estimate for the beamformer. In the presence of strong interference, detection is difficult. To overcome the effects of the interference, it is possible to use coherent integration of very long training sequences. However, that approach would be both computationally expensive and sensitive to channel stationarity. By first spatially whitening the received signal, the effect of the interference is mitigated allowing the use of relatively short training sequences. In the implemented receiver, the spatial whitening is achieved by using a QR decomposition and back-substitution.

1.2 Space-Time Coding

MIMO communication requires a space-time coding approach. Space-time coding techniques typically have strong connections to traditional forward error correction approaches. The field has been investigated widely. However, in the presence of interference, link performance is dominated by the receiver approach [6]. For the implementation discussed in this paper, a simple delay diversity encoding scheme is employed. A convolutionally encoded signal is transmitted from one transmit antenna while a delayed version of the signal is transmitted from a second antenna. While this space-time code is not particularly strong, it is easy to implement and provides complete spatial diversity.

2. Receiver Design

Two transmitters are used along with space-time coding to communicate with a four-channel receiver. The transmitted burst waveforms utilize QPSK modulations with pulse shaping for spectral confinement. A preamble is used to facilitate synchronization. As mentioned above, synchronization involves spatial whitening followed by matched-filtering to each transmitter's signature sequence. Matched filter outputs are combined to mitigate fading. The data portions of each waveform are bit-shifted versions of each other, providing full spatial diversity. Dual four-channel beamformers operating on the whitened data are used to separate the two transmitted waveforms. Three temporal taps are used in each spatial channel to provide equalization. The three temporal taps and four elements result in 12 total degrees of freedom that are adapted in a data-directed manner during the data portion of the waveforms. The two beamformer outputs are normalized and combined with bit delays to provide quasi-likelihood information for the decoder, which implements the IS-95A reverse channel rate 1/3 standard. Although the receiver is designed for burst waveforms, the implementation supports continuous transmission with distributed synchronization.

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3. Implementation

In implementing the MIMO receiver, hardware constraints were taken into account. Four Altera FPGAs of medium capacity are available for signal processing. A fifth FPGA is reserved strictly for routing signals between the FPGAs. Logic resources and maximum clock speed were the main limiting factors in this case as they are in most FPGA designs.

To optimize the allocation of logic resources, the design has been partitioned to fit into the four FPGAs as shown in Figure 3.1. FPGA 1 is the DIQ block which is assigned the task of converting data off the A/Ds to four channels of Inphase-Quarature samples, clocking at a data rate of 7 mega-samples per second. FPGA 2 accommodates the whitening block—a critical component for substantially reducing any strong interference prior to synchronization and beamforming. A synchronization process is performed in FPGA 3 using matched filtering to detect the start of each frame and send initial weight estimates to the beamforming block in FPGA 4. The output of the beamformer is then fed to a decoder residing in FPGA 3. The decoded output bits for an entire frame are sent out via USB to a PC for any further processing.

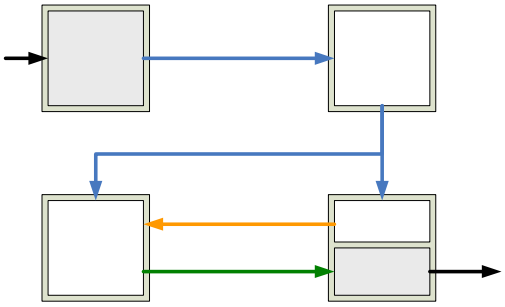

Figure 3.1 Signal processing in the MIMO receiver is divided into blocks spread across four FPGAs.

This project was done in coordination with Xetron Corporation. Xetron provided the hardware and the DIQ block. In addition, they were also working on the implementation of the transmitter. We were responsible for the receiver system design and coding of the MIMO receiver in VHDL. The decoder block is a standard Vitterbi decoder which can be purchased from a number of vendors as a core to be compiled into our design.

4. Testing and Performance

As of this writing, the code for the Whitening, Beamforming, and Synchronization blocks, together with code for synchronizing data among those blocks, have been written and tested. The analog front-end was not available for testing, so the actual DIQ block was replaced by a real-time emulator feeding out data, from a ROM, that resembled samples from a jamming scenario. The data were then processed in real-time through the remaining blocks as designed. Given that the Vitterbi decoder was not available, the beamformer output was sent to the PC via USB and was compared to MATLAB floating-point and fixed-point simulation. Tests showed that the Whitening, Beamformer, and Correlate/Sync blocks worked as designed. Figure 4.1 shows the hardware-extracted beamformer output matching with the expected signal from simulation. Subsequent decoding of this signal in Matlab yielded zero bit error. This step completed the verification of the core components of the receiver system.

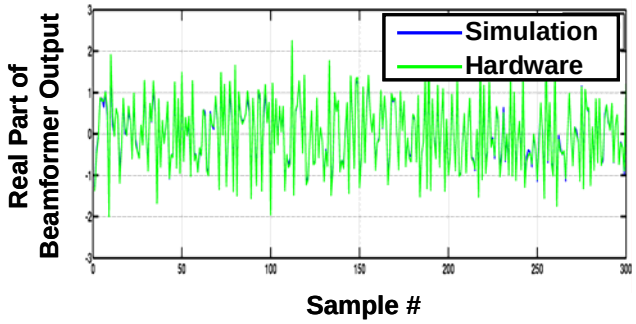

Figure 4.1 Output from beamformer block matches simulation

References

[1] G. J. Foschini, "Layered space-time architecture for wireless communication in a fading environment when using multi-element antennas," *Bell Labs Technical Journal*, vol. 1, no. 2, pp. 41–59, Autumn 1996.

[2] E. Telatar, "Capacity of multi-antenna Gaussian channels," *European Transactions on Telecommunications*, vol. 10, no. 6, pp. 585–595,November–December 1999.

[3] D. W. Bliss, A. M. Chan, and N. B. Chang, "MIMO wireless communication channel phenomenology," *IEEE Transactions on Antennas and Propagation*, vol. 52, no. 8, Aug. 2004.

[4] D. W. Bliss, K. W. Forsythe, A. O. Hero, and A. F. Yegulalp, "Environmental issues for MIMO capacity," *IEEE Transactions on Signal Processing*, vol. 50, no. 9, pp. 2128–2142, Sept. 2002.

[5] D. W. Bliss, "Robust MIMO wireless communication in the presence of interference using ad hoc antenna arrays," *Proceedings of MILCOM 03 (Boston)*, Oct. 2003.

[6] D. W. Bliss and K. W. Forsythe, "Information theoretic comparison of MIMO wireless communication receivers in the presence of interference," *Conference Record of the Thirty-Eighth Asilomar Conference on Signals, Systems & Computers*, Pacific Grove, Calif., Nov. 2004.