Application of Functional Coverage-Driven-Verification (CDV) Methodology to Real-Time Embedded Systems-on-Chip (SoC) for HW/SW State-Space Co-Verification and Architectural Exploration

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Next Generation State-of-the-art SoC (NG-SoC) designs implemented using 90/65 nm CMOS geometries will approach 25 millions gates of logic complexity and will include substantive integration of embedded memory (4-16 MB), and multiple instantiations of programmable CPU core (RISC, DSP, re-configurable) architectures. The implication is not only a fundamental redefinition of hardware and software architectural design trade-offs for fault-tolerant, High-Availability (HA), Real-Time (RT) systems, but a "paradigm-shift" in the verification methodology and development requirement for NG-SoCs, lest the result of unacceptable costly chip re-spins ($2M/65 nm re-spin) and time-to-market. The HW/SW interaction in NG-SoCs will only accentuate the already dominant project verification resource requirements (70-80%) for hardware and introduce a heretofore unseen HW/SW co-verification baseline.

The last 5 years of verification methodology innovation has resulted in the definition of Hardware Verification Languages (HVL, 'e', Vera®, SystemC Verification Library) and "Coverage-Driven-Verification" (CDV) methodologies that have transformed HW integrated circuit verification from traditional "manual directed" test environments, to fully-automated, self-checking verification sub-systems. Such Verification Process Automation (VPA) methodologies have achieved higher design implementation quality, verification predictability, and time-to–market improvement. However, in a practical sense, this wave of innovation has been limited to the hardware domain. Verification of software IP (destined to become the dominant resource component for NG-SoCs), be it module, platform, or system level has remained a directed task constrained to emulation or FPGA-based platforms and introduced late in the design flow or only after manufacture. Driven by customer demand and requirements, major Electronic Design Automation (EDA) companies have partnered with major systems providers to innovate new, leading-edge technologies and methodology that can apply CDV to HW/SW co-verification and architectural exploration for design trade-offs in NG-SoCs specifications.

While there are HW/SW co-simulation/development methodologies have been marketed over the last several years, these tools lack the close coupling between HW and SW interaction needed to effectively verify the system state-space and critical "corner case" scenarios that exist for BOTH the intra and inter-boundaries for/between the HW and SW components that constitute the architecture of NG-SoCs. Applying CDV techniques to the HW/SW problem facilitates a VPA of critical HW and SW critical state space scenarios. This redefined exploration of HW/SW verification will expose associated system architectural and implementation defects previously found by chance or after product deployment, introducing a heretofore unseen state-space exploration methodology.

This technical paper will define a CDV, System Verification Methodology (sVM), and introduce the concept of a SW modular, re-useable Verification Component (VC) for controlling, monitoring, and verifying SW in a manner similar to re-useable/modular HW Intellectual Property (IP) cores through a Generic Software Adapter (GSA). It will shown how CDA-based SW technology may be used for coupling the HW and SW verification environments for NG-SoCs verification and design. Such SW VC's form a common test environment capable of providing unprecedented coordination, control and monitoring for embedded RT SW drivers and HW abstraction layers via mixed simulation mechanisms such as the SystemC Transaction Layer Modelling (TLM) library, Register Transfer Languages (RTL, VHDL/Verilog), and accelerated/emulated environments, thus providing increased system simulation speeds needed for NG-SoC development. Such SW VC's are equally effective irrespective of embedded CPU core implementations (C++, SystemC-base ISS, RTL, or functional model executing as part of a hardware-based simulation acceleration or emulation engine). In addition, a thorough examination of how market-

available advanced CDV products, that allow communication with different simulation platforms and RTLs can take advantage of SW-driven CDV technology for HW/SW NG-SoC verification and design will be addressed. Finally, the schemas introduced in this paper require no modification or special hooks to the embedded processor models, whether those processor models are from 3rd party vendors or integrated with proprietary software development and debugging environments.